Aurelii Communications

Preliminary Data Sheet

PN Code Generator Peripheral (N=7)

Features:

- 3 bit Fibonacci Linear Feedback Shift Register
- Variable 3 bit Register Contents for Pseudorandom (PN) Sequence Bank 0
- 28 Channel Serial PN Code Output Bank 0
- Global Output Enable for all PN Code Channels
- Local Output Enable for each PN Code Channel
- Global Enable for all PN Code Channels
- Local Enable for each PN Code Channel
- 5 bit Address and 16 bit Microprocessor Interface
  - 4 bit Control and Status Register
  - 3 bit PN Read back
  - Global Enable
  - Global Output Enable
- 4 bit Output for FIFO Interface
  - 3 bit PN Sequence Register
  - 1 bit PN Output

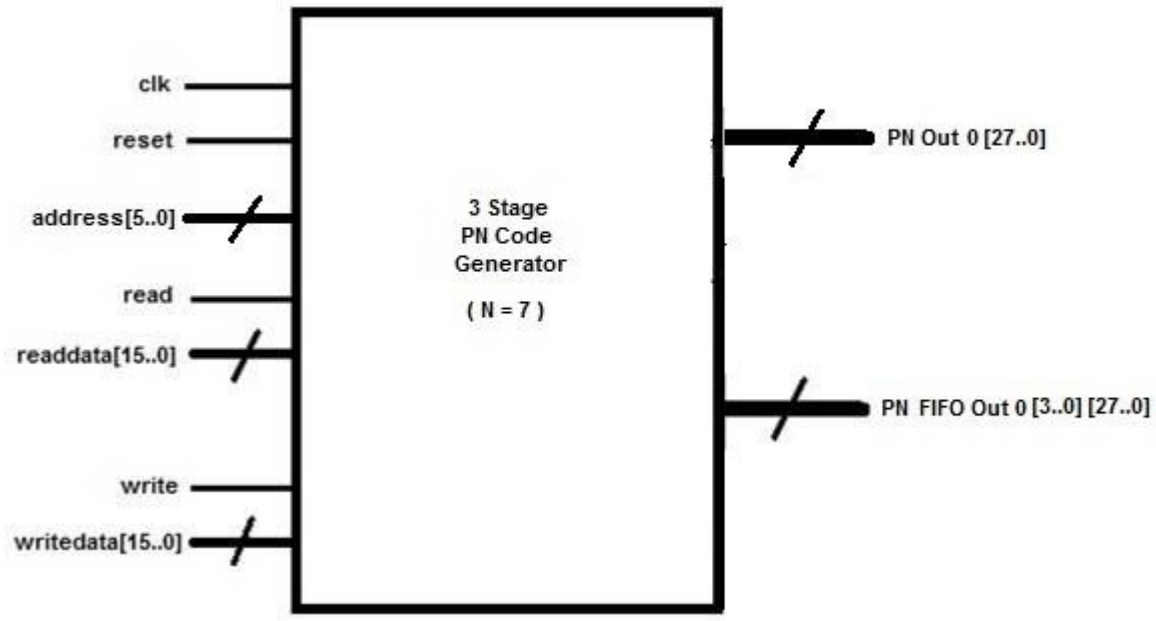

Figure 1: 3 Stage PN Code Generator (N = 7) Block Diagram

Introduction

Pseudo Noise (PN) sequences are flexible code types used for a variety of secure communication methods. The most widely used application of PN Sequences is Wireless communications. This includes both Cellular and Satellite communications. The uses of PN Sequences extend far beyond Wireless communications to a variety of applications in Voice, Video, and Data transmission over a wide range of communication channel types.

PN Sequence Configurations

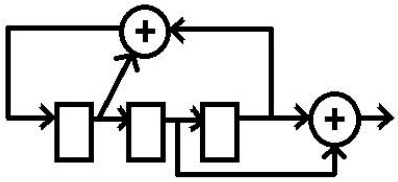

Figure 2a

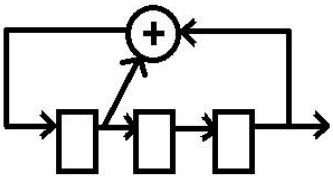

Figure 2b

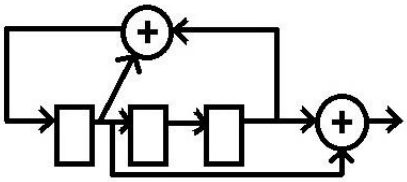

Figure 2c

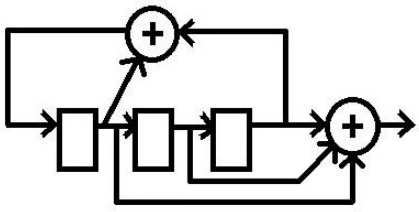

Figure 2d

Figure 2: 3 Stage Fibonacci Linear Feedback Shift Register (LFSR) PN Sequence Generators

Table 1: LFSR Register Contents and PN Output Sequences Corresponding to Figure 2

Table 1a

	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output
Seed	111	0	110	0	101	1	010	1	100	1	001	0	011	1
	110	0	101	1	010	1	100	1	001	0	011	1	111	0
	101	1	010	1	100	1	001	0	011	1	111	0	110	0
	010	1	100	1	001	0	011	1	111	0	110	0	101	1
	100	1	001	0	011	1	111	0	110	0	101	1	010	1
	001	0	011	1	111	0	110	0	101	1	010	1	100	1
	011	1	111	0	110	0	101	1	010	1	100	1	001	0

Table 1b

	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output
Seed	111	1	110	1	101	1	010	0	100	1	001	0	011	0
	110	1	101	1	010	0	100	1	001	0	011	0	111	1
	101	1	010	0	100	1	001	0	011	0	111	1	110	1
	010	0	100	1	001	0	011	0	111	1	110	1	101	1
	100	1	001	0	011	0	111	1	110	1	101	1	010	0
	001	0	011	0	111	1	110	1	101	1	010	0	100	1
	011	0	111	1	110	1	101	1	010	0	100	1	001	0

Table 1c

	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output
Seed	111	0	110	1	101	0	010	0	100	1	001	1	011	1
	110	1	101	0	010	0	100	1	001	1	011	1	111	0
	101	0	010	0	100	1	001	1	011	1	111	0	110	1
	010	0	100	1	001	1	011	1	111	0	110	1	101	0
	100	1	001	1	011	1	111	0	110	1	101	0	010	0
	001	1	011	1	111	0	110	1	101	0	010	0	100	1
	011	1	111	0	110	1	101	0	010	0	100	1	001	1

Table 1d

	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output	PN Register [2..0]	Output
Seed	111	1	110	0	101	0	010	1	100	1	001	1	011	0
	110	0	101	0	010	1	100	1	001	1	011	0	111	1
	101	0	010	1	100	1	001	1	011	0	111	1	110	0
	010	1	100	1	001	1	011	0	111	1	110	0	101	0
	100	1	001	1	011	0	111	1	110	0	101	0	010	1
	001	1	011	0	111	1	110	0	101	0	010	1	100	1
	011	0	111	1	110	0	101	0	010	1	100	1	001	1

PN Sequence Waveforms

Figure 2 shows the output waveforms for the 28 channel serial output of the PN Code Generator Peripheral. The channels labeled PN0 – PN27 shown in Figure 2 correspond to the ports labeled PN0 – PN27 on the peripheral block diagram of Figure 2. Each channel contains a register that can be accessed through the microprocessor interface. This allows the user to create 28 unique codes; 1 for each channel. The clock waveform shown in the simulation is the chip clock.

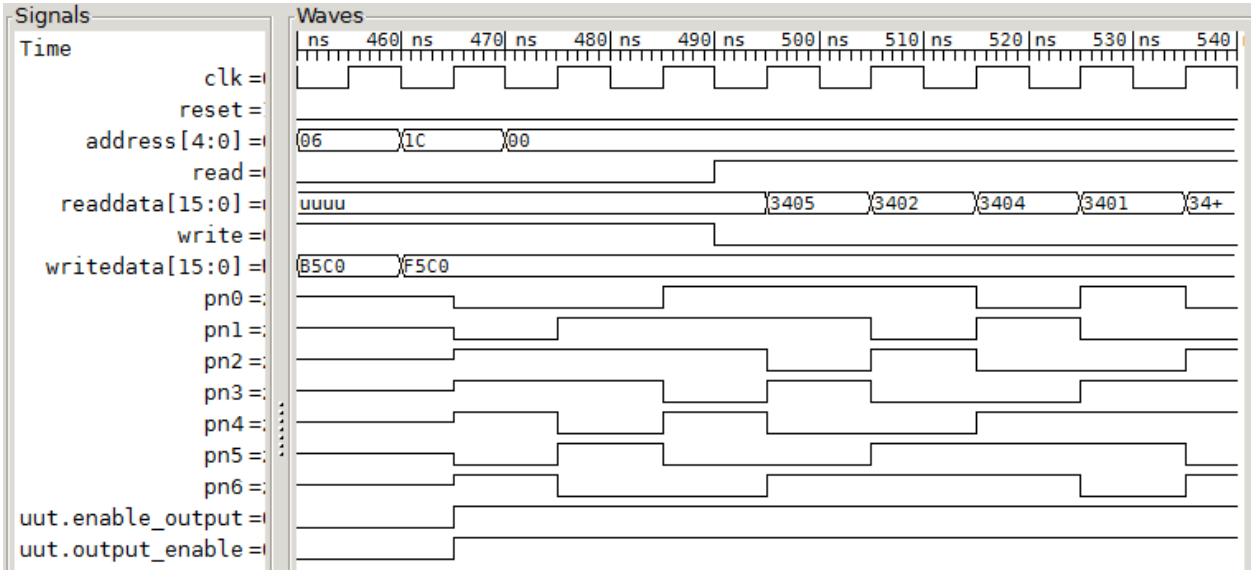

Figure 3a: Output Waveforms corresponding to Table 1a[1]

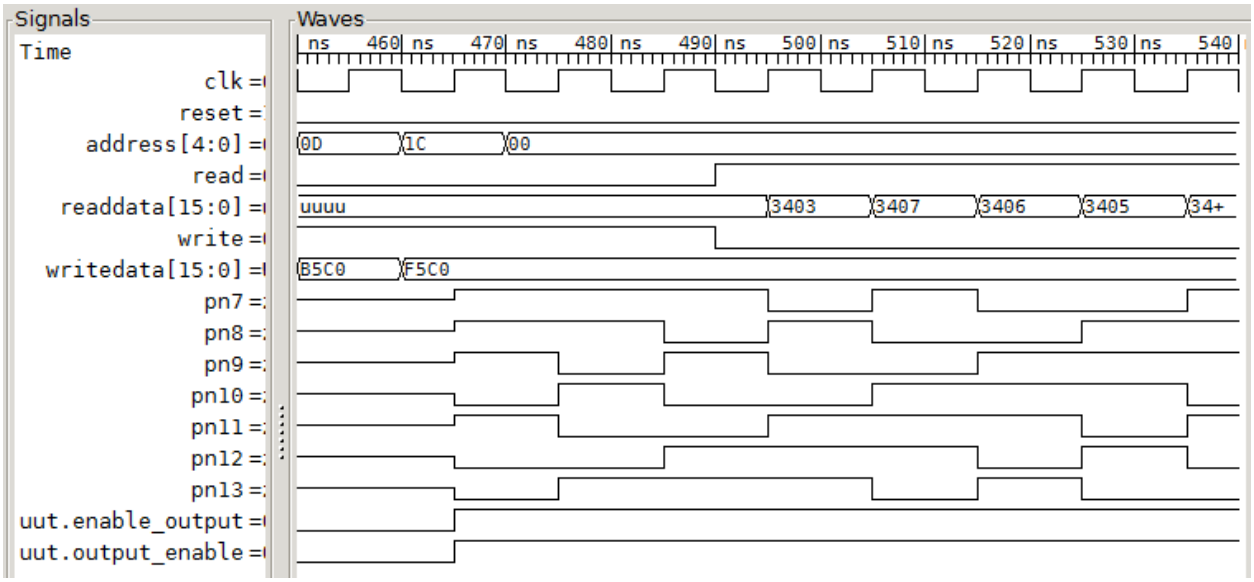

Figure 3b: Output Waveforms corresponding to Table 1b[1]

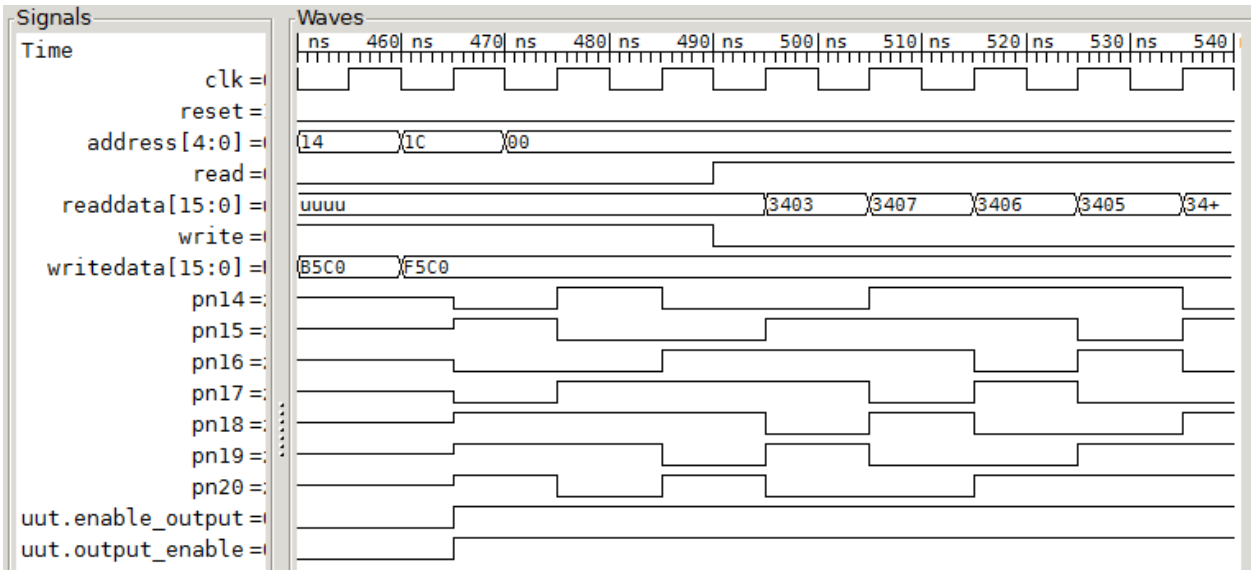

Figure 3c: Output Waveforms corresponding to Table 1c[1]

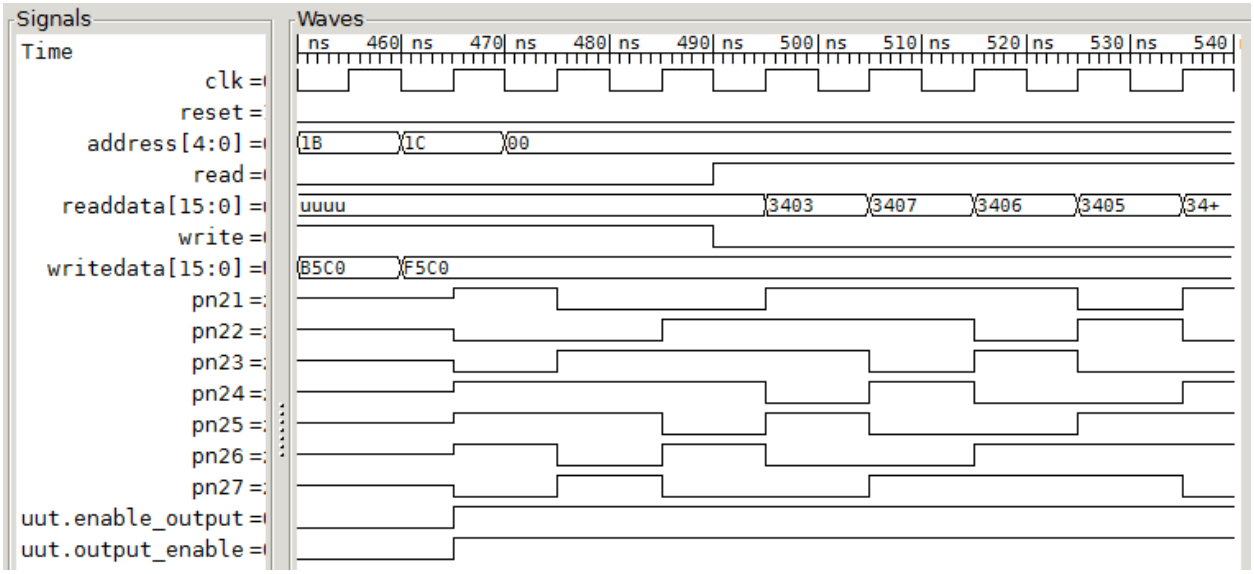

Figure 3d: Output Waveforms corresponding to Table 1d[1]

Notes:

1. PN[27..0] of Output Waveforms correspond to PN[28..1] of Cross Correlation Data

Initial Contents of PN Registers

The initial contents of the PN registers upon System Reset are shown in the Table 2.

PN Register Initial Contents		
Group	Register	Seed
1	0	001
	1	010
	2	011
	3	100
	4	101
	5	110
	6	111
	7	001
2	8	010
	9	011
	10	100
	11	101
	12	110
	13	111
3	14	001
	15	010
	16	011
	17	100
	18	101
	19	110
	20	111
4	21	001
	22	010
	23	011
	24	100
	25	101
	26	110
	27	111

Table 2: Initial Contents of PN Registers

PN Register Microprocessor Interface

Tables 3 Illustrates the Address map for read and write transfers to the PN Registers.

PN Register Addresses		
Group	Register	Address
1	0	0
	1	1
	2	2
	3	3
	4	4
	5	5
	6	6
	7	7
2	8	8
	9	9
	10	A
	11	B
	12	C
	13	D
3	14	E
	15	F
	16	10
	17	11
	18	12
	19	13
	20	14
4	21	15
	22	16
	23	17
	24	18
	25	19
	26	1A
	27	1B

Table 3: Address Table for PN Registers [1][2][3]

Notes:

1. For write transfers to the PN Registers, reg_init_enable located at address 1D must be written with a value of 1. To disable write transfers to the PN registers, reg_init_enable located at address 1D must be written with a value of 0. reg_init_enable is accessed using writedata[9].
2. For write transfers, the PN Registers are accessed using writedata[2..0]
3. For read transfers, the PN Registers are accessed using readdata[2..0]

Microprocessor Interface

The 7 ports of the microprocessor interface for the Gold Code Peripheral are shown below.

reset	-	Peripheral reset
clk	-	Chip Clock
address	-	5 bit address (bits 4 down to 0) for accessing peripheral registers
write	-	Register write enable
writedata	-	16 bit write data (bits 15 down to 0) for peripheral registers
read	-	Register read enable
readdata	-	16 bit read data (bits 15 down to 0) for peripheral registers

Writing to the peripheral registers requires

1) The write address be present on address[4:0]
2) The write data be present on writedata[15:0]
3) The write enable be asserted

Reading from the peripheral registers requires

1) The read address be present on address[4:0]
2) The read data be present on readdata[15:0]
3) The read enable be asserted

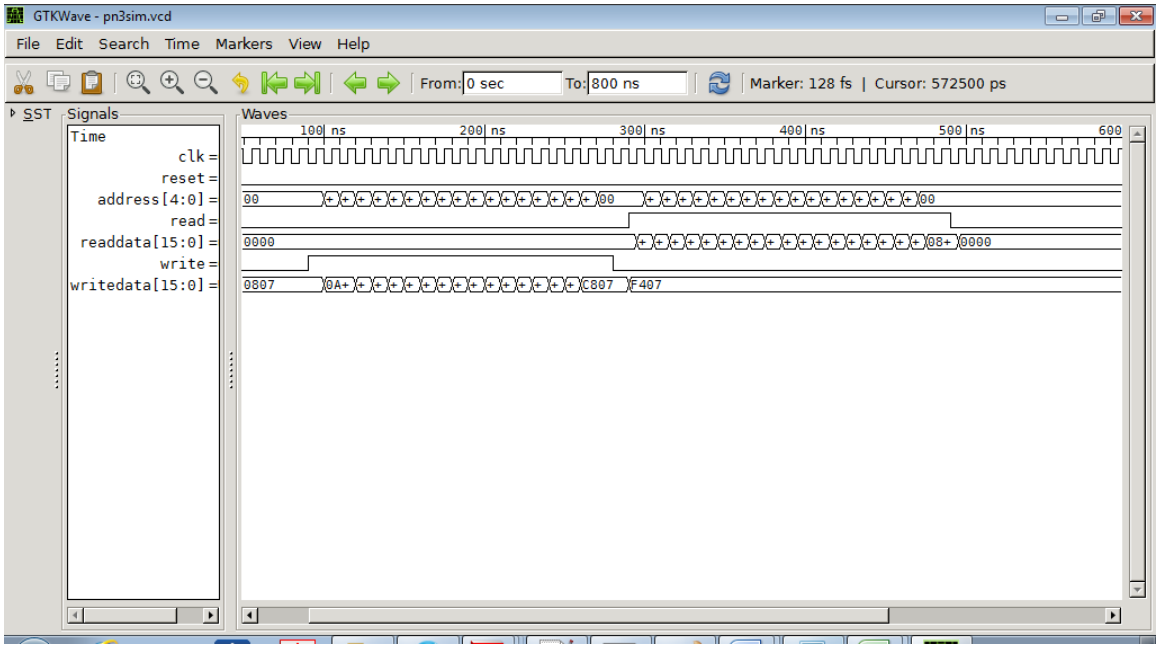

Figure 4: Microprocessor Interface

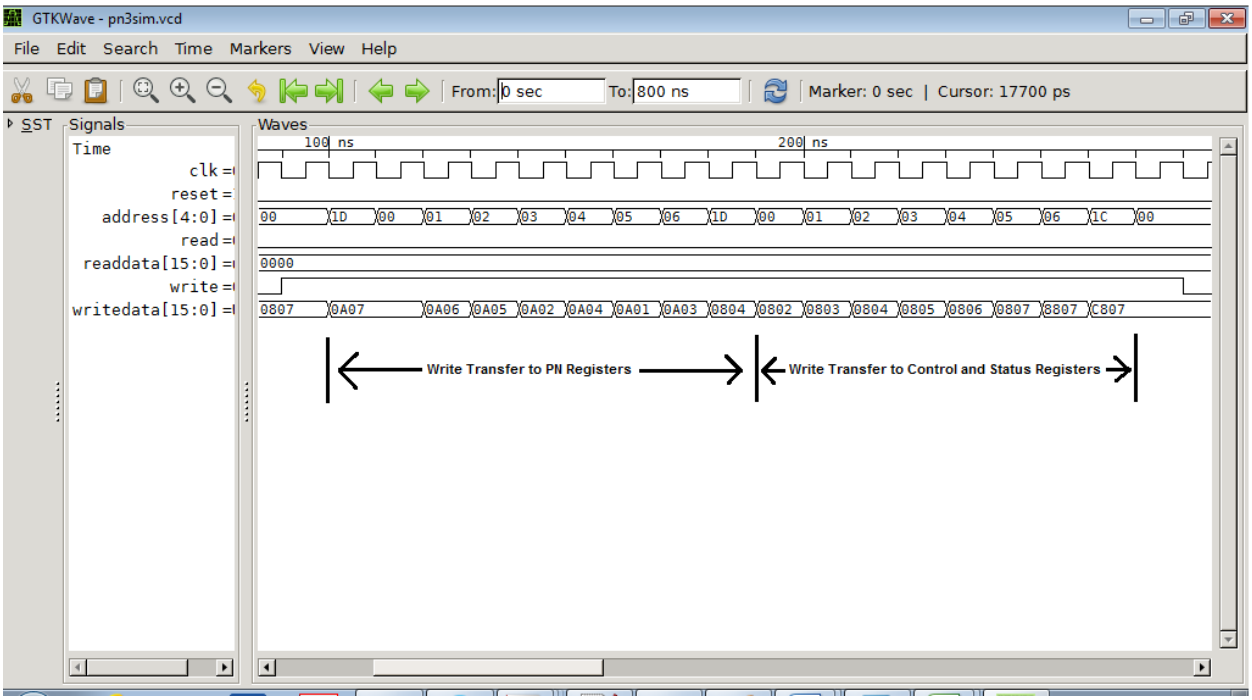

Figure 5: Write Transfer Detailed View

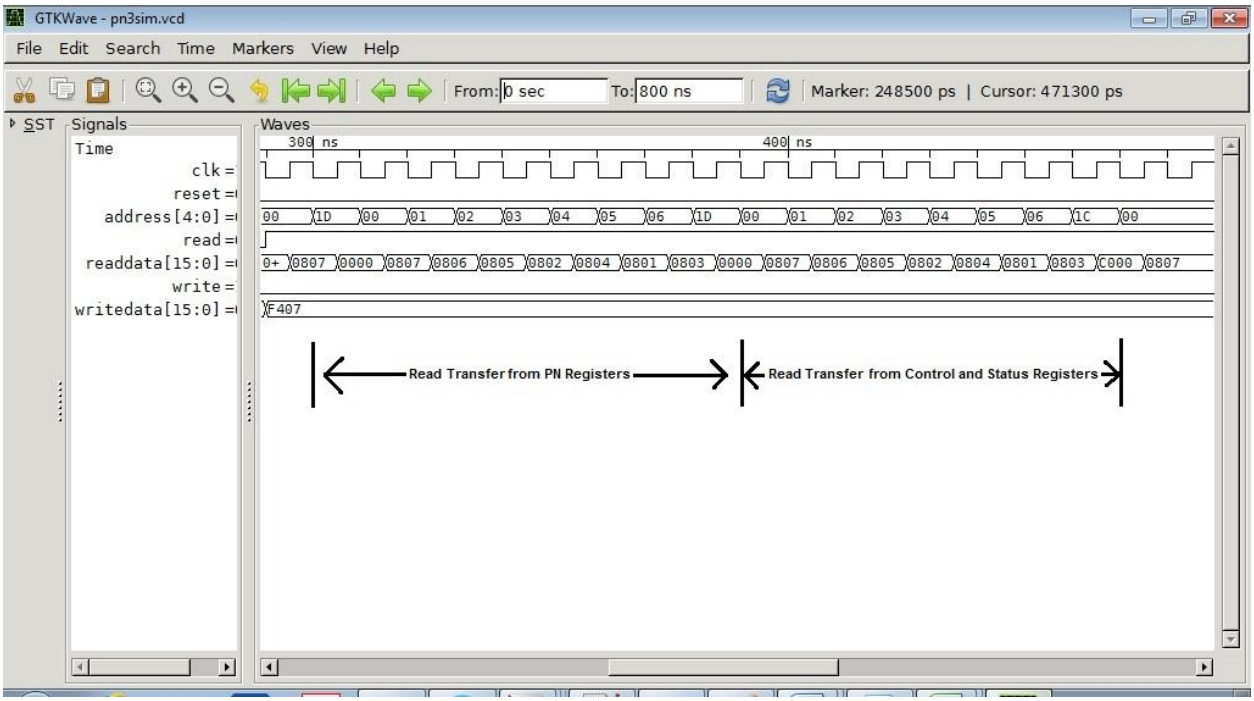

Figure 6: Read Transfer Detailed View

Clock Enable

Each PN Code channel can be enabled individually or as a group. The control and status register (CSR) of each PN Code channel has 2 bits that controls the enable of that channel. CSR[0] is the Asynchronous Clock Enable and CSR[2] is the synchronous Clock Enable. There is also an enable that controls all 28 PN Code channels called enable_output. The default setting for both the CSR enables for each channel and the enable that controls all 28 channels is disabled. The user can set the CSR enables and then set the enable that controls all 28 channels to enable the PN Code channels as a group. The user can also set the enable that controls all 28 channels and then set the CSR enables that control the individual channels to enable each individual channel respectively.

Figure 3 shows the PN Code channels being enabled as a group. The signal name for the Clock Enable in the simulation is enable_output. Figure 7 shows the PN Codes channels being enabled individually.

Output Enable

Each PN Code channel pin can be tri stated individually or as a group. The control and status register (CSR) of each PN Code channel has a bit that controls the output enable of that channel. CSR[3] is the Channel Output Enable. There is also an output enable that controls the output of all 28 PN Code channels. The default setting for both the CSR output enable for each channel and the output enable that controls all 28 channels is disabled. The user can set the CSR output enables and then set the output enable that controls all 28 channels to tri state the PN Code channels as a group. The user can also set the output enable that controls all 28 channels and then set the CSR output enable that controls the individual channels to tri state each individual channel respectively.

Figure 3 shows the PN Code channels being tri-stated as a group. Figure 7 shows the PN Codes channels being tri-stated individually.

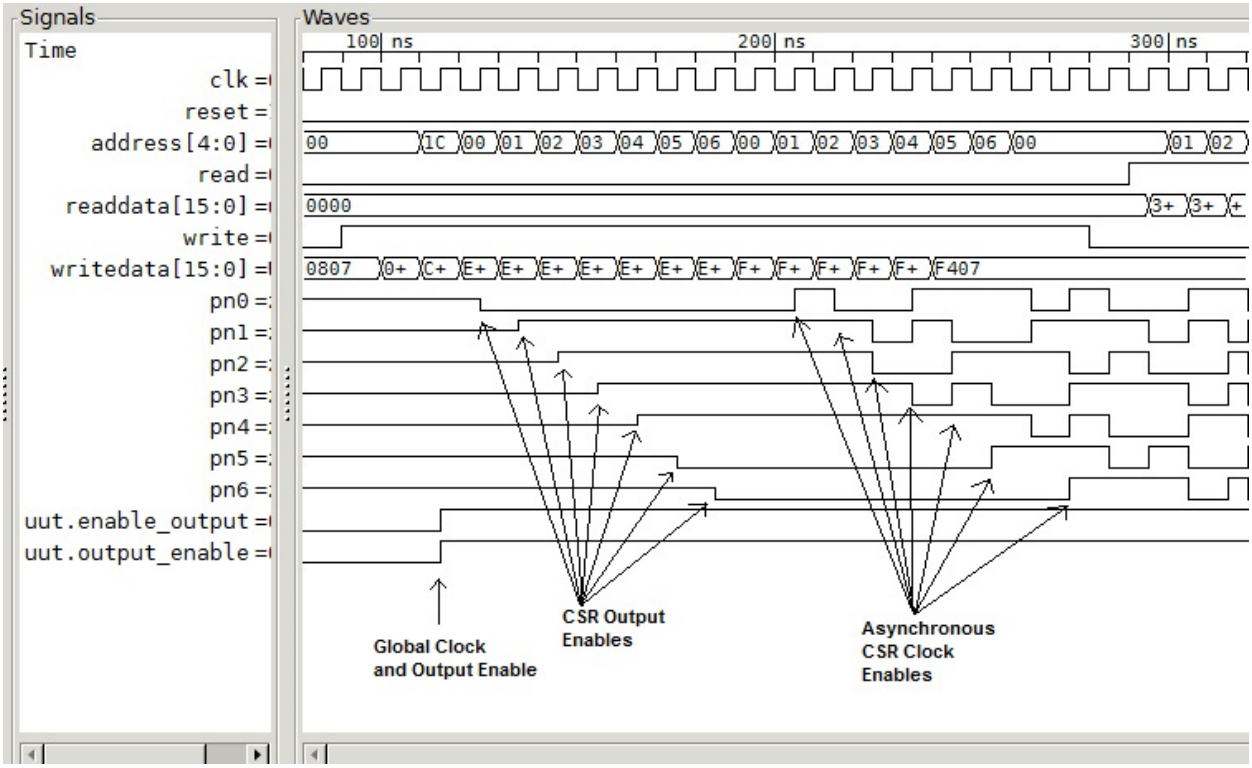

Figure 7: CSR Output Enables and Clock Enables

First In First Out (FIFO) Interface

The PN Code Module has a 4 bit Output FIFO interface. The FIFO interface can be connected to the input of a FIFO buffer. The bits are organized as shown below:

[3]	PN Code Output Register
[2..0]	PN Registers

This allows the user to examine the contents of the PN Code generator while the PN Code channel output is running.

The output of the FIFO buffer may be used to interface to a Direct Memory Access (DMA) Controller.

Figure 8 shows the parallel FIFO output interface for a single channel (PN 0). Figure 9 shows the parallel FIFO outputs for the 7 channels of Group 1 (PN 0 – PN 7).

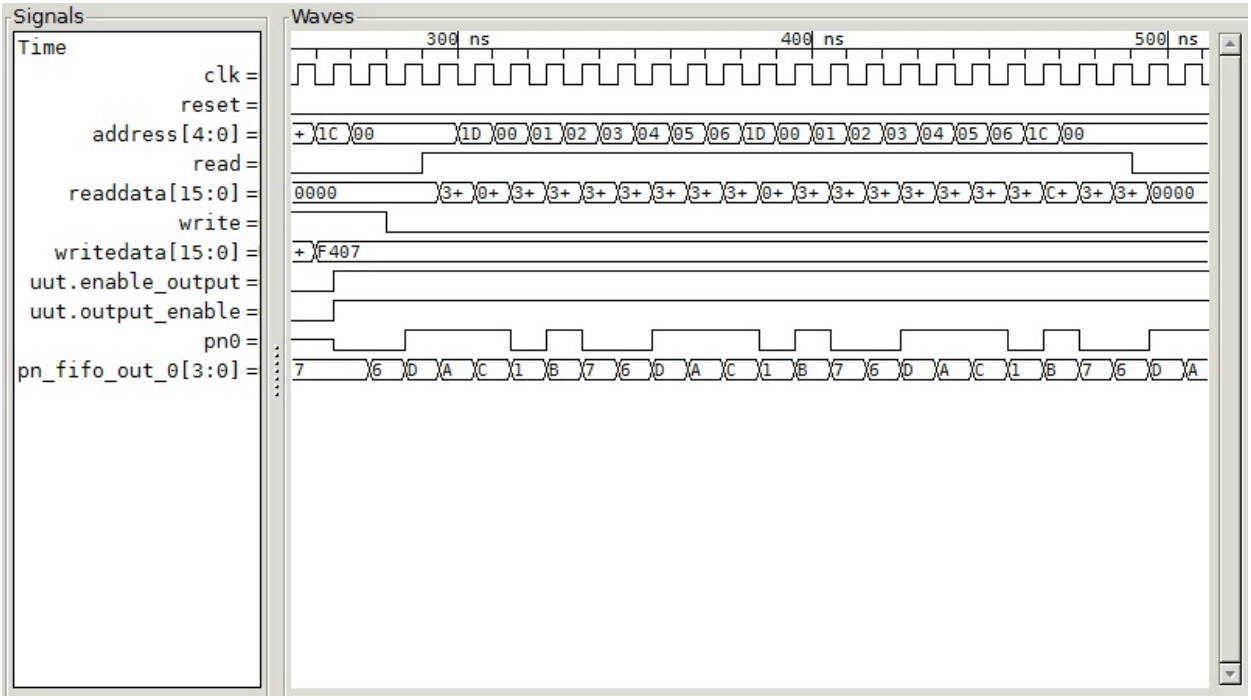

Figure 8: PN 0 FIFO Output

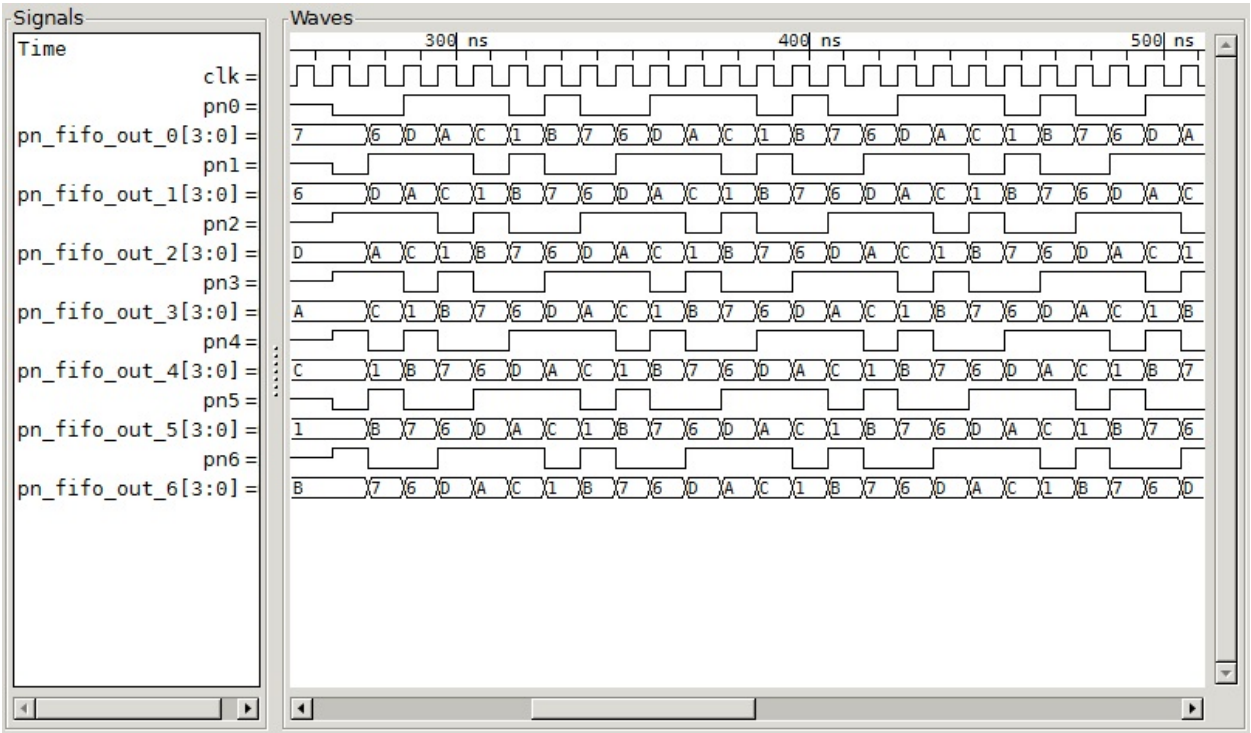

Figure 9: Group 1 FIFO Outputs (PN 0 – PN6)

Port Declarations

Port	Width	Description
CLK	1	Chip Clock
RESET	1	Peripheral Reset
ADDRESS	5	Peripheral Address
READ	1	Read Enable
READDATA	16	Read Data
WRITE	1	Write Enable
WRITEDATA	16	Write Data
PN_FIFO_OUT_0	4	Channel 0 FIFO Output
PN_FIFO_OUT_1	4	Channel 1 FIFO Output
PN_FIFO_OUT_2	4	Channel 2 FIFO Output
PN_FIFO_OUT_3	4	Channel 3 FIFO Output
PN_FIFO_OUT_4	4	Channel 4 FIFO Output
PN_FIFO_OUT_5	4	Channel 5 FIFO Output
PN_FIFO_OUT_6	4	Channel 6 FIFO Output
PN_FIFO_OUT_7	4	Channel 7 FIFO Output
PN_FIFO_OUT_8	4	Channel 8 FIFO Output
PN_FIFO_OUT_9	4	Channel 9 FIFO Output
PN_FIFO_OUT_10	4	Channel 10 FIFO Output
PN_FIFO_OUT_11	4	Channel 11 FIFO Output
PN_FIFO_OUT_12	4	Channel 12 FIFO Output
PN_FIFO_OUT_13	4	Channel 13 FIFO Output
PN_FIFO_OUT_14	4	Channel 14 FIFO Output
PN_FIFO_OUT_15	4	Channel 15 FIFO Output
PN_FIFO_OUT_16	4	Channel 16 FIFO Output
PN_FIFO_OUT_17	4	Channel 17 FIFO Output
PN_FIFO_OUT_18	4	Channel 18 FIFO Output
PN_FIFO_OUT_19	4	Channel 19 FIFO Output
PN_FIFO_OUT_20	4	Channel 20 FIFO Output
PN_FIFO_OUT_21	4	Channel 21 FIFO Output
PN_FIFO_OUT_22	4	Channel 22 FIFO Output
PN_FIFO_OUT_23	4	Channel 23 FIFO Output
PN_FIFO_OUT_24	4	Channel 24 FIFO Output
PN_FIFO_OUT_25	4	Channel 25 FIFO Output
PN_FIFO_OUT_26	4	Channel 26 FIFO Output
PN_FIFO_OUT_27	4	Channel 27 FIFO Output
PN0	1	Channel 0 PN Code Output
PN1	1	Channel 1 PN Code Output
PN2	1	Channel 2 PN Code Output
PN3	1	Channel 3 PN Code Output
PN4	1	Channel 4 PN Code Output
PN5	1	Channel 5 PN Code Output
PN6	1	Channel 6 PN Code Output
PN7	1	Channel 7 PN Code Output
PN8	1	Channel 8 PN Code Output
PN9	1	Channel 9 PN Code Output
PN10	1	Channel 10 PN Code Output
PN11	1	Channel 11 PN Code Output
PN12	1	Channel 12 PN Code Output
PN13	1	Channel 13 PN Code Output
PN14	1	Channel 14 PN Code Output
PN15	1	Channel 15 PN Code Output
PN16	1	Channel 16 PN Code Output
PN17	1	Channel 17 PN Code Output
PN18	1	Channel 18 PN Code Output
PN19	1	Channel 19 PN Code Output
PN20	1	Channel 20 PN Code Output
PN21	1	Channel 21 PN Code Output
PN22	1	Channel 22 PN Code Output
PN23	1	Channel 23 PN Code Output
PN24	1	Channel 24 PN Code Output
PN25	1	Channel 25 PN Code Output
PN26	1	Channel 26 PN Code Output
PN27	1	Channel 27 PN Code Output

Table 4: Peripheral Port Descriptions

Address Tables

Register Address Map (Write)																
Address / Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	Unused	Unused	CSR[0][3]	CSR[0][2]	CSR[0][1]	CSR[0][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[0][2]	PN[0][1]	PN[0][0]
0x1	Unused	Unused	CSR[1][3]	CSR[1][2]	CSR[1][1]	CSR[1][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[1][2]	PN[1][1]	PN[1][0]
0x2	Unused	Unused	CSR[2][3]	CSR[2][2]	CSR[2][1]	CSR[2][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[2][2]	PN[2][1]	PN[2][0]
0x3	Unused	Unused	CSR[3][3]	CSR[3][2]	CSR[3][1]	CSR[3][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[3][2]	PN[3][1]	PN[3][0]
0x4	Unused	Unused	CSR[4][3]	CSR[4][2]	CSR[4][1]	CSR[4][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[4][2]	PN[4][1]	PN[4][0]
0x5	Unused	Unused	CSR[5][3]	CSR[5][2]	CSR[5][1]	CSR[5][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[5][2]	PN[5][1]	PN[5][0]
0x6	Unused	Unused	CSR[6][3]	CSR[6][2]	CSR[6][1]	CSR[6][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[6][2]	PN[6][1]	PN[6][0]
0x7	Unused	Unused	CSR[7][3]	CSR[7][2]	CSR[7][1]	CSR[7][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[7][2]	PN[7][1]	PN[7][0]
0x8	Unused	Unused	CSR[8][3]	CSR[8][2]	CSR[8][1]	CSR[8][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[8][2]	PN[8][1]	PN[8][0]
0x9	Unused	Unused	CSR[9][3]	CSR[9][2]	CSR[9][1]	CSR[9][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[9][2]	PN[9][1]	PN[9][0]
0xA	Unused	Unused	CSR[10][3]	CSR[10][2]	CSR[10][1]	CSR[10][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[10][2]	PN[10][1]	PN[10][0]
0xB	Unused	Unused	CSR[11][3]	CSR[11][2]	CSR[11][1]	CSR[11][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[11][2]	PN[11][1]	PN[11][0]
0xC	Unused	Unused	CSR[12][3]	CSR[12][2]	CSR[12][1]	CSR[12][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[12][2]	PN[12][1]	PN[12][0]
0xD	Unused	Unused	CSR[13][3]	CSR[13][2]	CSR[13][1]	CSR[13][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[13][2]	PN[13][1]	PN[13][0]
0xE	Unused	Unused	CSR[14][3]	CSR[14][2]	CSR[14][1]	CSR[14][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[14][2]	PN[14][1]	PN[14][0]
0xF	Unused	Unused	CSR[15][3]	CSR[15][2]	CSR[15][1]	CSR[15][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[15][2]	PN[15][1]	PN[15][0]
0x10	Unused	Unused	CSR[16][3]	CSR[16][2]	CSR[16][1]	CSR[16][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[16][2]	PN[16][1]	PN[16][0]
0x11	Unused	Unused	CSR[17][3]	CSR[17][2]	CSR[17][1]	CSR[17][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[17][2]	PN[17][1]	PN[17][0]
0x12	Unused	Unused	CSR[18][3]	CSR[18][2]	CSR[18][1]	CSR[18][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[18][2]	PN[18][1]	PN[18][0]
0x13	Unused	Unused	CSR[19][3]	CSR[19][2]	CSR[19][1]	CSR[19][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[19][2]	PN[19][1]	PN[19][0]
0x14	Unused	Unused	CSR[20][3]	CSR[20][2]	CSR[20][1]	CSR[20][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[20][2]	PN[20][1]	PN[20][0]
0x15	Unused	Unused	CSR[21][3]	CSR[21][2]	CSR[21][1]	CSR[21][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[21][2]	PN[21][1]	PN[21][0]
0x16	Unused	Unused	CSR[22][3]	CSR[22][2]	CSR[22][1]	CSR[22][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[22][2]	PN[22][1]	PN[22][0]
0x17	Unused	Unused	CSR[23][3]	CSR[23][2]	CSR[23][1]	CSR[23][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[23][2]	PN[23][1]	PN[23][0]
0x18	Unused	Unused	CSR[24][3]	CSR[24][2]	CSR[24][1]	CSR[24][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[24][2]	PN[24][1]	PN[24][0]
0x19	Unused	Unused	CSR[25][3]	CSR[25][2]	CSR[25][1]	CSR[25][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[25][2]	PN[25][1]	PN[25][0]
0x1A	Unused	Unused	CSR[26][3]	CSR[26][2]	CSR[26][1]	CSR[26][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[26][2]	PN[26][1]	PN[26][0]
0X1B	Unused	Unused	CSR[27][3]	CSR[27][2]	CSR[27][1]	CSR[27][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[27][2]	PN[27][1]	PN[27][0]
0x1C	OE	CE	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused
0x1D	Unused	Unused	Unused	Unused	Unused	Unused	reg_init_enable	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused

Table 5: Register Address Map for Write Transfers

Register Address Map (Read)																
Address / Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	Unused	Unused	CSR[0][3]	CSR[0][2]	CSR[0][1]	CSR[0][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[0][2]	PN[0][1]	PN[0][0]
0x1	Unused	Unused	CSR[1][3]	CSR[1][2]	CSR[1][1]	CSR[1][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[1][2]	PN[1][1]	PN[1][0]
0x2	Unused	Unused	CSR[2][3]	CSR[2][2]	CSR[2][1]	CSR[2][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[2][2]	PN[2][1]	PN[2][0]
0x3	Unused	Unused	CSR[3][3]	CSR[3][2]	CSR[3][1]	CSR[3][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[3][2]	PN[3][1]	PN[3][0]
0x4	Unused	Unused	CSR[4][3]	CSR[4][2]	CSR[4][1]	CSR[4][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[4][2]	PN[4][1]	PN[4][0]
0x5	Unused	Unused	CSR[5][3]	CSR[5][2]	CSR[5][1]	CSR[5][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[5][2]	PN[5][1]	PN[5][0]
0x6	Unused	Unused	CSR[6][3]	CSR[6][2]	CSR[6][1]	CSR[6][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[6][2]	PN[6][1]	PN[6][0]
0x7	Unused	Unused	CSR[7][3]	CSR[7][2]	CSR[7][1]	CSR[7][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[7][2]	PN[7][1]	PN[7][0]
0x8	Unused	Unused	CSR[8][3]	CSR[8][2]	CSR[8][1]	CSR[8][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[8][2]	PN[8][1]	PN[8][0]
0x9	Unused	Unused	CSR[9][3]	CSR[9][2]	CSR[9][1]	CSR[9][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[9][2]	PN[9][1]	PN[9][0]
0xA	Unused	Unused	CSR[10][3]	CSR[10][2]	CSR[10][1]	CSR[10][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[10][2]	PN[10][1]	PN[10][0]
0xB	Unused	Unused	CSR[11][3]	CSR[11][2]	CSR[11][1]	CSR[11][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[11][2]	PN[11][1]	PN[11][0]
0xC	Unused	Unused	CSR[12][3]	CSR[12][2]	CSR[12][1]	CSR[12][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[12][2]	PN[12][1]	PN[12][0]
0xD	Unused	Unused	CSR[13][3]	CSR[13][2]	CSR[13][1]	CSR[13][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[13][2]	PN[13][1]	PN[13][0]
0xE	Unused	Unused	CSR[14][3]	CSR[14][2]	CSR[14][1]	CSR[14][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[14][2]	PN[14][1]	PN[14][0]
0xF	Unused	Unused	CSR[15][3]	CSR[15][2]	CSR[15][1]	CSR[15][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[15][2]	PN[15][1]	PN[15][0]
0x10	Unused	Unused	CSR[16][3]	CSR[16][2]	CSR[16][1]	CSR[16][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[16][2]	PN[16][1]	PN[16][0]
0x11	Unused	Unused	CSR[17][3]	CSR[17][2]	CSR[17][1]	CSR[17][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[17][2]	PN[17][1]	PN[17][0]
0x12	Unused	Unused	CSR[18][3]	CSR[18][2]	CSR[18][1]	CSR[18][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[18][2]	PN[18][1]	PN[18][0]
0x13	Unused	Unused	CSR[19][3]	CSR[19][2]	CSR[19][1]	CSR[19][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[19][2]	PN[19][1]	PN[19][0]
0x14	Unused	Unused	CSR[20][3]	CSR[20][2]	CSR[20][1]	CSR[20][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[20][2]	PN[20][1]	PN[20][0]
0x15	Unused	Unused	CSR[21][3]	CSR[21][2]	CSR[21][1]	CSR[21][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[21][2]	PN[21][1]	PN[21][0]
0x16	Unused	Unused	CSR[22][3]	CSR[22][2]	CSR[22][1]	CSR[22][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[22][2]	PN[22][1]	PN[22][0]
0x17	Unused	Unused	CSR[23][3]	CSR[23][2]	CSR[23][1]	CSR[23][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[23][2]	PN[23][1]	PN[23][0]
0x18	Unused	Unused	CSR[24][3]	CSR[24][2]	CSR[24][1]	CSR[24][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[24][2]	PN[24][1]	PN[24][0]
0x19	Unused	Unused	CSR[25][3]	CSR[25][2]	CSR[25][1]	CSR[25][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[25][2]	PN[25][1]	PN[25][0]
0x1A	Unused	Unused	CSR[26][3]	CSR[26][2]	CSR[26][1]	CSR[26][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[26][2]	PN[26][1]	PN[26][0]
0X1B	Unused	Unused	CSR[27][3]	CSR[27][2]	CSR[27][1]	CSR[27][0]	Unused	Unused	Unused	Unused	Unused	Unused	Unused	PN[27][2]	PN[27][1]	PN[27][0]
0x1C	OE	CE	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused
0x1D	Unused	Unused	Unused	Unused	Unused	Unused	reg_init_enable	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused

Table 6: Register Address Map for Read Transfers

Register Definitions - Control and Status Registers

CSR[27:0][3:0] - 28 Channel 4 Bit Control and Status Register

CSR[0][3] - Channel 0 Bit 3 (Channel 0 Output Enable)
CSR[0][2] - Channel 0 Bit 2 (Channel 0 Channel Enable)
CSR[0][1] - Channel 0 Bit 1 (Channel 0 Synchronous Reset)
CSR[0][0] - Channel 0 Bit 0 (Channel 0 Clock Enable)

CSR[1][3] - Channel 1 Bit 3 (Channel 1 Output Enable)
CSR[1][2] - Channel 1 Bit 2 (Channel 1 Channel Enable)
CSR[1][1] - Channel 1 Bit 1 (Channel 1 Synchronous Reset)
CSR[1][0] - Channel 1 Bit 0 (Channel 1 Clock Enable)

CSR[2][3] - Channel 2 Bit 3 (Channel 2 Output Enable)
CSR[2][2] - Channel 2 Bit 2 (Channel 2 Channel Enable)
CSR[2][1] - Channel 2 Bit 1 (Channel 2 Synchronous Reset)
CSR[2][0] - Channel 2 Bit 0 (Channel 2 Clock Enable)

CSR[3][3] - Channel 3 Bit 3 (Channel 3 Output Enable)
CSR[3][2] - Channel 3 Bit 2 (Channel 3 Channel Enable)
CSR[3][1] - Channel 3 Bit 1 (Channel 3 Synchronous Reset)
CSR[3][0] - Channel 3 Bit 0 (Channel 3 Clock Enable)

CSR[4][3] - Channel 4 Bit 3 (Channel 4 Output Enable)
CSR[4][2] - Channel 4 Bit 2 (Channel 4 Channel Enable)
CSR[4][1] - Channel 4 Bit 1 (Channel 4 Synchronous Reset)
CSR[4][0] - Channel 4 Bit 0 (Channel 4 Clock Enable)

CSR[5][3] - Channel 5 Bit 3 (Channel 5 Output Enable)
CSR[5][2] - Channel 5 Bit 2 (Channel 5 Channel Enable)
CSR[5][1] - Channel 5 Bit 1 (Channel 5 Synchronous Reset)
CSR[5][0] - Channel 5 Bit 0 (Channel 5 Clock Enable)

CSR[6][3] - Channel 6 Bit 3 (Channel 6 Output Enable)
CSR[6][2] - Channel 6 Bit 2 (Channel 6 Channel Enable)
CSR[6][1] - Channel 6 Bit 1 (Channel 6 Synchronous Reset)
CSR[6][0] - Channel 6 Bit 0 (Channel 6 Clock Enable)

Register Definitions - Control and Status Registers

CSR[27:0][3:0] - 28 Channel 4 Bit Control and Status Register

CSR[7][3] - Channel 7 Bit 3 (Channel 7 Output Enable)
CSR[7][2] - Channel 7 Bit 2 (Channel 7 Channel Enable)
CSR[7][1] - Channel 7 Bit 1 (Channel 7 Synchronous Reset)
CSR[7][0] - Channel 7 Bit 0 (Channel 7 Clock Enable)

CSR[8][3] - Channel 8 Bit 3 (Channel 8 Output Enable)
CSR[8][2] - Channel 8 Bit 2 (Channel 8 Channel Enable)
CSR[8][1] - Channel 8 Bit 1 (Channel 8 Synchronous Reset)
CSR[8][0] - Channel 8 Bit 0 (Channel 8 Clock Enable)

CSR[9][3] - Channel 9 Bit 3 (Channel 9 Output Enable)
CSR[9][2] - Channel 9 Bit 2 (Channel 9 Channel Enable)
CSR[9][1] - Channel 9 Bit 1 (Channel 9 Synchronous Reset)
CSR[9][0] - Channel 9 Bit 0 (Channel 9 Clock Enable)

CSR[10][3] - Channel 10 Bit 3 (Channel 10 Output Enable)
CSR[10][2] - Channel 10 Bit 2 (Channel 10 Channel Enable)
CSR[10][1] - Channel 10 Bit 1 (Channel 10 Synchronous Reset)
CSR[10][0] - Channel 10 Bit 0 (Channel 10 Clock Enable)

CSR[11][3] - Channel 11 Bit 3 (Channel 11 Output Enable)
CSR[11][2] - Channel 11 Bit 2 (Channel 11 Channel Enable)
CSR[11][1] - Channel 11 Bit 1 (Channel 11 Synchronous Reset)
CSR[11][0] - Channel 11 Bit 0 (Channel 11 Clock Enable)

CSR[12][3] - Channel 12 Bit 3 (Channel 12 Output Enable)
CSR[12][2] - Channel 12 Bit 2 (Channel 12 Channel Enable)
CSR[12][1] - Channel 12 Bit 1 (Channel 12 Synchronous Reset)
CSR[12][0] - Channel 12 Bit 0 (Channel 12 Clock Enable)

CSR[13][3] - Channel 13 Bit 3 (Channel 13 Output Enable)
CSR[13][2] - Channel 13 Bit 2 (Channel 13 Channel Enable)
CSR[13][1] - Channel 13 Bit 1 (Channel 13 Synchronous Reset)
CSR[13][0] - Channel 13 Bit 0 (Channel 13 Clock Enable)

Register Definitions - Control and Status Registers

CSR[27:0][3:0] - 28 Channel 4 Bit Control and Status Register

CSR[14][3] - Channel 14 Bit 3 (Channel 14 Output Enable)
CSR[14][2] - Channel 14 Bit 2 (Channel 14 Channel Enable)
CSR[14][1] - Channel 14 Bit 1 (Channel 14 Synchronous Reset)
CSR[14][0] - Channel 14 Bit 0 (Channel 14 Clock Enable)

CSR[15][3] - Channel 15 Bit 3 (Channel 15 Output Enable)
CSR[15][2] - Channel 15 Bit 2 (Channel 15 Channel Enable)
CSR[15][1] - Channel 15 Bit 1 (Channel 15 Synchronous Reset)
CSR[15][0] - Channel 15 Bit 0 (Channel 15 Clock Enable)

CSR[16][3] - Channel 16 Bit 3 (Channel 16 Output Enable)
CSR[16][2] - Channel 16 Bit 2 (Channel 16 Channel Enable)
CSR[16][1] - Channel 16 Bit 1 (Channel 16 Synchronous Reset)
CSR[16][0] - Channel 16 Bit 0 (Channel 16 Clock Enable)

CSR[17][3] - Channel 17 Bit 3 (Channel 17 Output Enable)
CSR[17][2] - Channel 17 Bit 2 (Channel 17 Channel Enable)
CSR[17][1] - Channel 17 Bit 1 (Channel 17 Synchronous Reset)
CSR[17][0] - Channel 17 Bit 0 (Channel 17 Clock Enable)

CSR[18][3] - Channel 18 Bit 3 (Channel 18 Output Enable)
CSR[18][2] - Channel 18 Bit 2 (Channel 18 Channel Enable)
CSR[18][1] - Channel 18 Bit 1 (Channel 18 Synchronous Reset)
CSR[18][0] - Channel 18 Bit 0 (Channel 18 Clock Enable)

CSR[19][3] - Channel 19 Bit 3 (Channel 19 Output Enable)
CSR[19][2] - Channel 19 Bit 2 (Channel 19 Channel Enable)
CSR[19][1] - Channel 19 Bit 1 (Channel 19 Synchronous Reset)
CSR[19][0] - Channel 19 Bit 0 (Channel 19 Clock Enable)

CSR[20][3] - Channel 20 Bit 3 (Channel 20 Output Enable)
CSR[20][2] - Channel 20 Bit 2 (Channel 20 Channel Enable)
CSR[20][1] - Channel 20 Bit 1 (Channel 20 Synchronous Reset)
CSR[20][0] - Channel 20 Bit 0 (Channel 20 Clock Enable)

Register Definitions - Control and Status Registers

CSR[27:0][3:0] - 28 Channel 4 Bit Control and Status Register

CSR[21][3] - Channel 21 Bit 3 (Channel 21 Output Enable)
CSR[21][2] - Channel 21 Bit 2 (Channel 21 Channel Enable)
CSR[21][1] - Channel 21 Bit 1 (Channel 21 Synchronous Reset)
CSR[21][0] - Channel 21 Bit 0 (Channel 21 Clock Enable)

CSR[22][3] - Channel 22 Bit 3 (Channel 22 Output Enable)
CSR[22][2] - Channel 22 Bit 2 (Channel 22 Channel Enable)
CSR[22][1] - Channel 22 Bit 1 (Channel 22 Synchronous Reset)
CSR[22][0] - Channel 22 Bit 0 (Channel 22 Clock Enable)

CSR[23][3] - Channel 23 Bit 3 (Channel 23 Output Enable)
CSR[23][2] - Channel 23 Bit 2 (Channel 23 Channel Enable)
CSR[23][1] - Channel 23 Bit 1 (Channel 23 Synchronous Reset)
CSR[23][0] - Channel 23 Bit 0 (Channel 23 Clock Enable)

CSR[24][3] - Channel 24 Bit 3 (Channel 24 Output Enable)
CSR[24][2] - Channel 24 Bit 2 (Channel 24 Channel Enable)
CSR[24][1] - Channel 24 Bit 1 (Channel 24 Synchronous Reset)
CSR[24][0] - Channel 24 Bit 0 (Channel 24 Clock Enable)

CSR[25][3] - Channel 25 Bit 3 (Channel 25 Output Enable)
CSR[25][2] - Channel 25 Bit 2 (Channel 25 Channel Enable)
CSR[25][1] - Channel 25 Bit 1 (Channel 25 Synchronous Reset)
CSR[25][0] - Channel 25 Bit 0 (Channel 25 Clock Enable)

CSR[26][3] - Channel 26 Bit 3 (Channel 26 Output Enable)
CSR[26][2] - Channel 26 Bit 2 (Channel 26 Channel Enable)
CSR[26][1] - Channel 26 Bit 1 (Channel 26 Synchronous Reset)
CSR[26][0] - Channel 26 Bit 0 (Channel 26 Clock Enable)

CSR[27][3] - Channel 27 Bit 3 (Channel 27 Output Enable)
CSR[27][2] - Channel 27 Bit 2 (Channel 27 Channel Enable)
CSR[27][1] - Channel 27 Bit 1 (Channel 27 Synchronous Reset)
CSR[27][0] - Channel 27 Bit 0 (Channel 27 Clock Enable)

Register Definitions - Pseudo Noise (PN) Sequence Registers

Group 1

PN[0][2]	-	Channel 0 / Bit 2
PN[0][1]	-	Channel 0 / Bit 1
PN[0][0]	-	Channel 0 / Bit 0
PN[1][2]	-	Channel 1 / Bit 2
PN[1][1]	-	Channel 1 / Bit 1
PN[1][0]	-	Channel 1 / Bit 0
PN[2][2]	-	Channel 2 / Bit 2
PN[2][1]	-	Channel 2 / Bit 1
PN[2][0]	-	Channel 2 / Bit 0
PN[3][2]	-	Channel 3 / Bit 2
PN[3][1]	-	Channel 3 / Bit 1
PN[3][0]	-	Channel 3 / Bit 0
PN[4][2]	-	Channel 4 / Bit 2
PN[4][1]	-	Channel 4 / Bit 1
PN[4][0]	-	Channel 4 / Bit 0
PN[5][2]	-	Channel 5 / Bit 2
PN[5][1]	-	Channel 5 / Bit 1
PN[5][0]	-	Channel 5 / Bit 0
PN[6][2]	-	Channel 6 / Bit 2
PN[6][1]	-	Channel 6 / Bit 1
PN[6][0]	-	Channel 6 / Bit 0

Register Definitions - Pseudo Noise (PN) Sequence Registers

Group 2

PN[7][2]	-	Channel 7 / Bit 2
PN[7][1]	-	Channel 7 / Bit 1
PN[7][0]	-	Channel 7 / Bit 0
PN[8][2]	-	Channel 8 / Bit 2
PN[8][1]	-	Channel 8 / Bit 1
PN[8][0]	-	Channel 8 / Bit 0
PN[9][2]	-	Channel 9 / Bit 2
PN[9][1]	-	Channel 9 / Bit 1
PN[9][0]	-	Channel 9 / Bit 0
PN[10][2]	-	Channel 10 / Bit 2
PN[10][1]	-	Channel 10 / Bit 1
PN[10][0]	-	Channel 10 / Bit 0
PN[11][2]	-	Channel 11 / Bit 2
PN[11][1]	-	Channel 11 / Bit 1
PN[11][0]	-	Channel 11 / Bit 0
PN[12][2]	-	Channel 12 / Bit 2
PN[12][1]	-	Channel 12 / Bit 1
PN[12][0]	-	Channel 12 / Bit 0
PN[13][2]	-	Channel 13 / Bit 2
PN[13][1]	-	Channel 13 / Bit 1
PN[13][0]	-	Channel 13 / Bit 0

Register Definitions - Pseudo Noise (PN) Sequence Register

Group 3

PN[14][2]	-	Channel 14 / Bit 2
PN[14][1]	-	Channel 14 / Bit 1
PN[14][0]	-	Channel 14 / Bit 0
PN[15][2]	-	Channel 15 / Bit 2
PN[15][1]	-	Channel 15 / Bit 1
PN[15][0]	-	Channel 15 / Bit 0
PN[16][2]	-	Channel 16 / Bit 2
PN[16][1]	-	Channel 16 / Bit 1
PN[16][0]	-	Channel 16 / Bit 0
PN[17][2]	-	Channel 17 / Bit 2
PN[17][1]	-	Channel 17 / Bit 1
PN[17][0]	-	Channel 17 / Bit 0
PN[18][2]	-	Channel 18 / Bit 2
PN[18][1]	-	Channel 18 / Bit 1
PN[18][0]	-	Channel 18 / Bit 0
PN[19][2]	-	Channel 19 / Bit 2
PN[19][1]	-	Channel 19 / Bit 1
PN[19][0]	-	Channel 19 / Bit 0
PN[20][2]	-	Channel 20 / Bit 2
PN[20][1]	-	Channel 20 / Bit 1
PN[20][0]	-	Channel 20 / Bit 0

Register Definitions - Pseudo Noise (PN) Sequence Register

Group 4

PN[21][2]	-	Channel 21 / Bit 2
PN[21][1]	-	Channel 21 / Bit 1
PN[21][0]	-	Channel 21 / Bit 0
PN[22][2]	-	Channel 22 / Bit 2
PN[22][1]	-	Channel 22 / Bit 1
PN[22][0]	-	Channel 22 / Bit 0
PN[23][2]	-	Channel 23 / Bit 2
PN[23][1]	-	Channel 23 / Bit 1
PN[23][0]	-	Channel 23 / Bit 0
PN[24][2]	-	Channel 24 / Bit 2
PN[24][1]	-	Channel 24 / Bit 1
PN[24][0]	-	Channel 24 / Bit 0
PN[25][2]	-	Channel 25 / Bit 2
PN[25][1]	-	Channel 25 / Bit 1
PN[25][0]	-	Channel 25 / Bit 0
PN[26][2]	-	Channel 26 / Bit 2
PN[26][1]	-	Channel 26 / Bit 1
PN[26][0]	-	Channel 26 / Bit 0
PN[27][2]	-	Channel 27 / Bit 2
PN[27][1]	-	Channel 27 / Bit 1
PN[27][0]	-	Channel 27 / Bit 0

Register Definitions - Global Registers

OE	-	Global Output Enable
CE	-	Global Clock Enable
REG_INIT_ENABLE	-	PN Write Initialization

Aurelii Communications

Preliminary Data Sheet

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 1

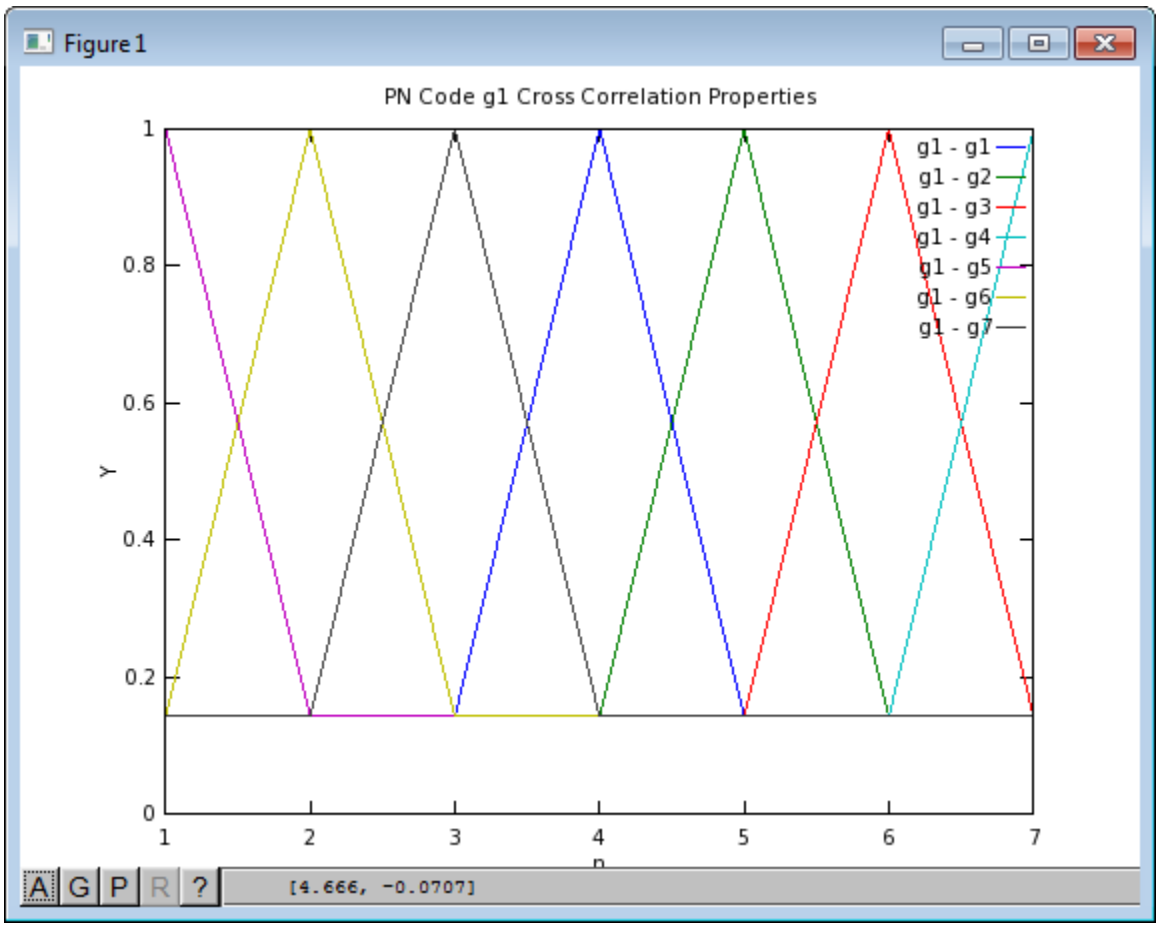

Figure 1: PN Sequence g1 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 1

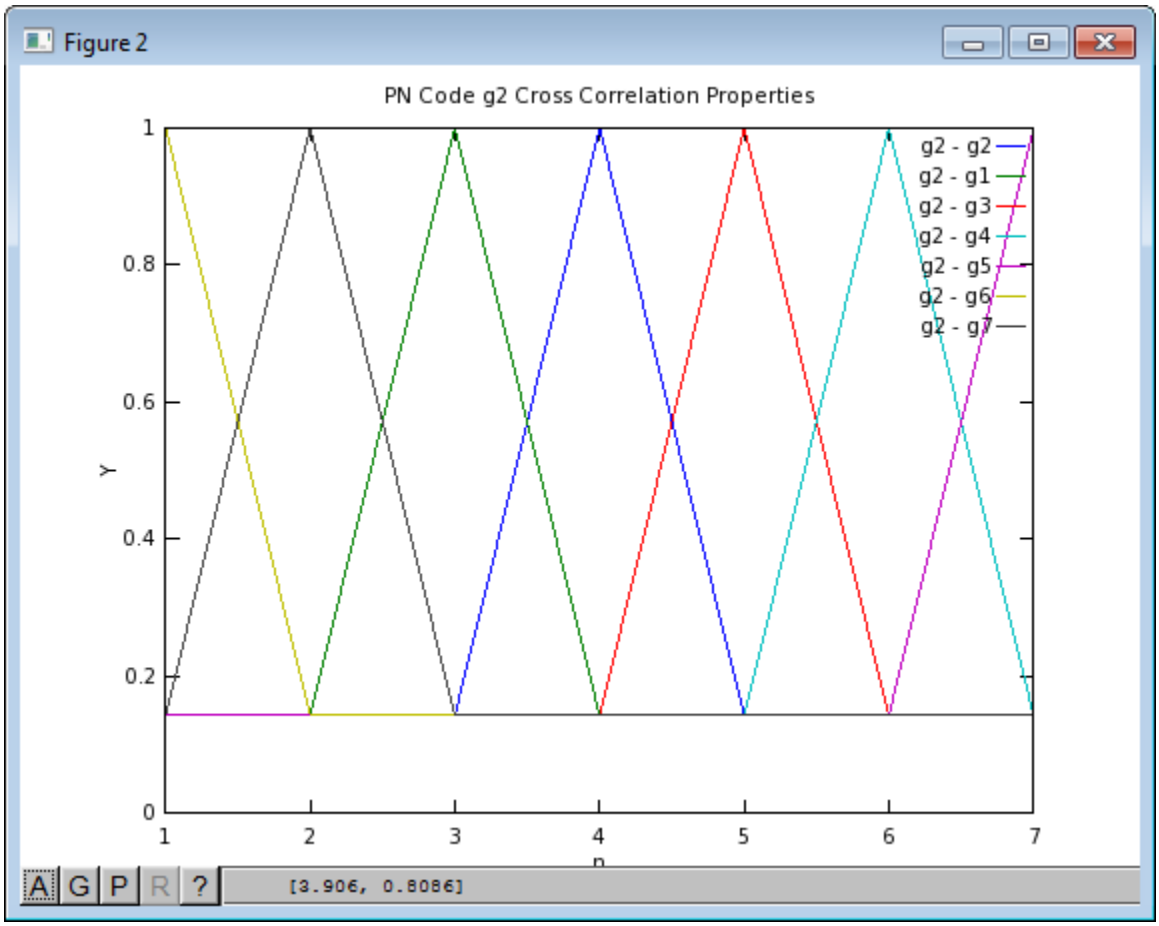

Figure 2: PN Sequence g2 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 1

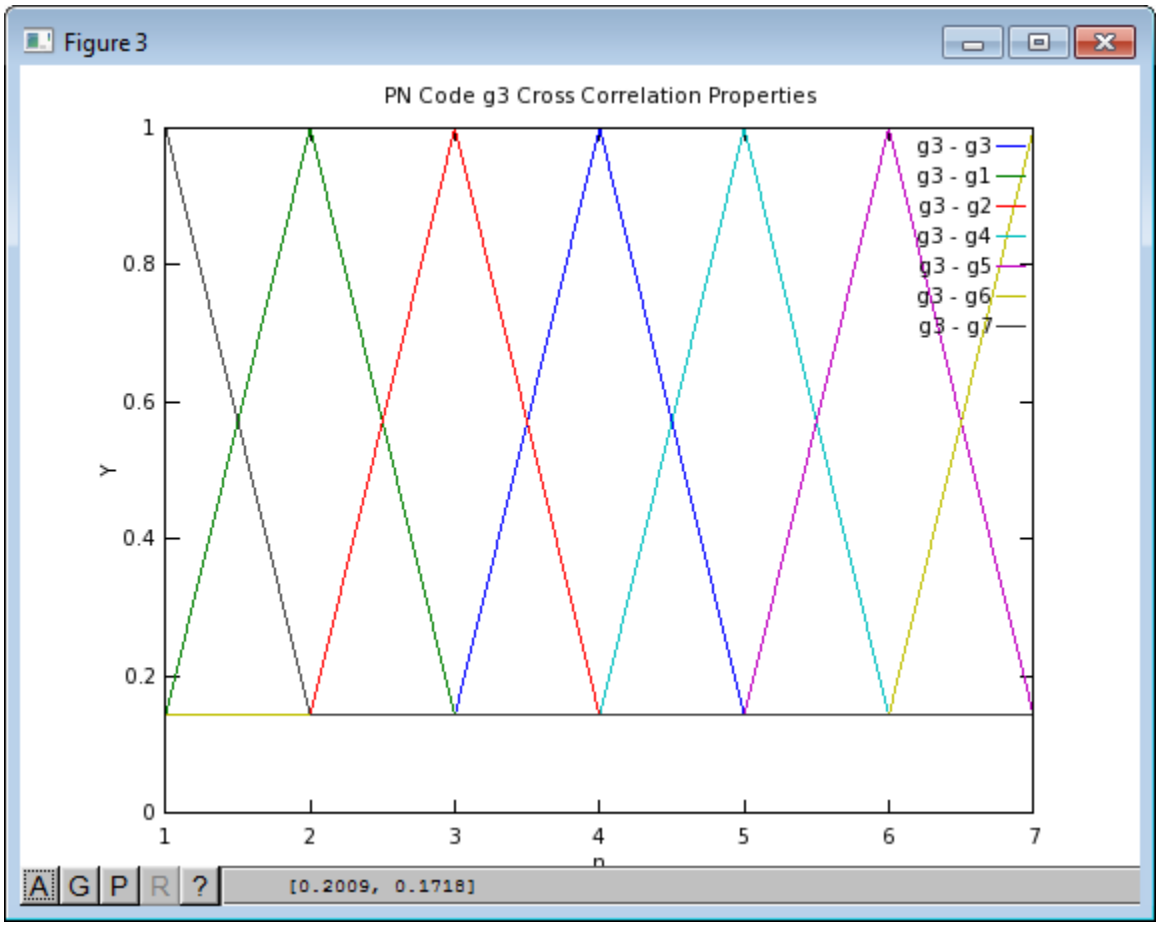

Figure 3: PN Sequence g3 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 1

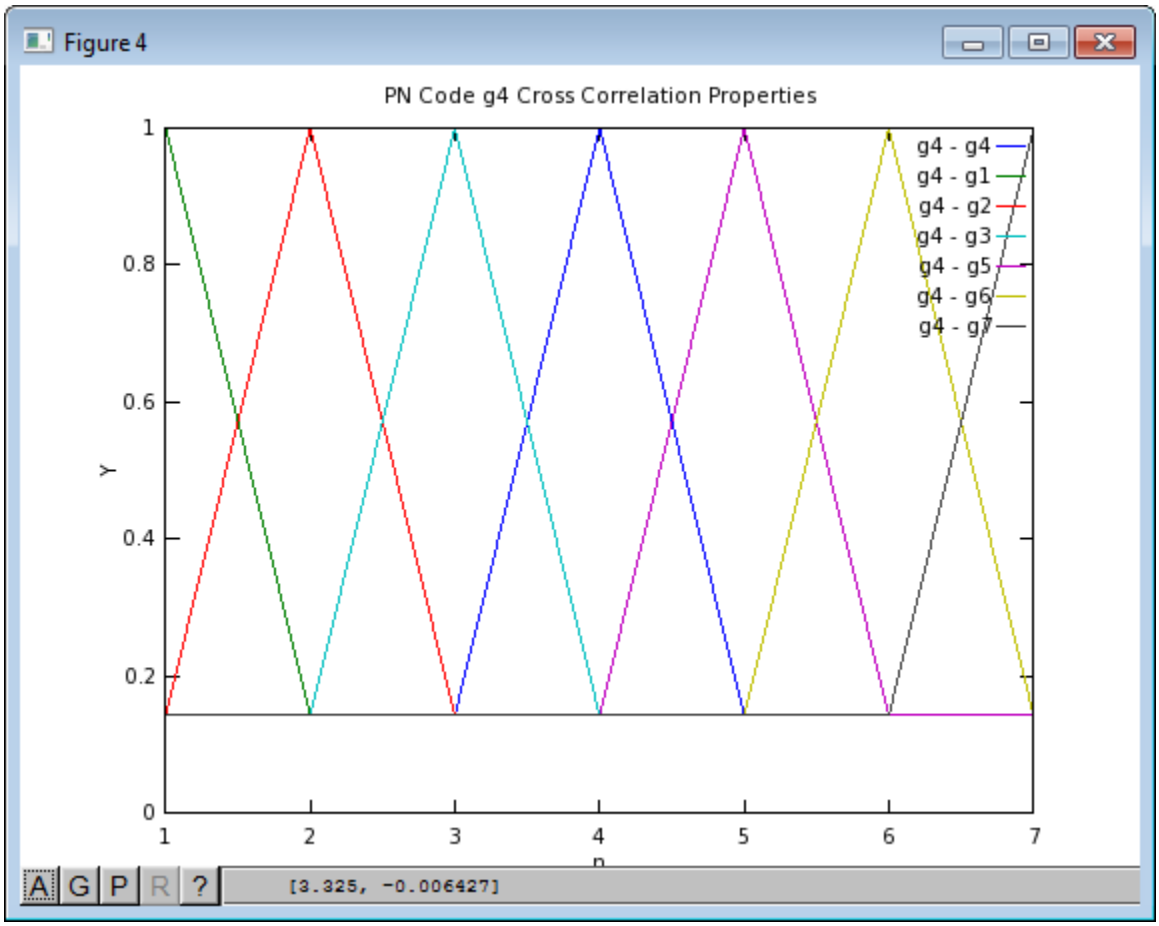

Figure 4: PN Sequence g4 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 1

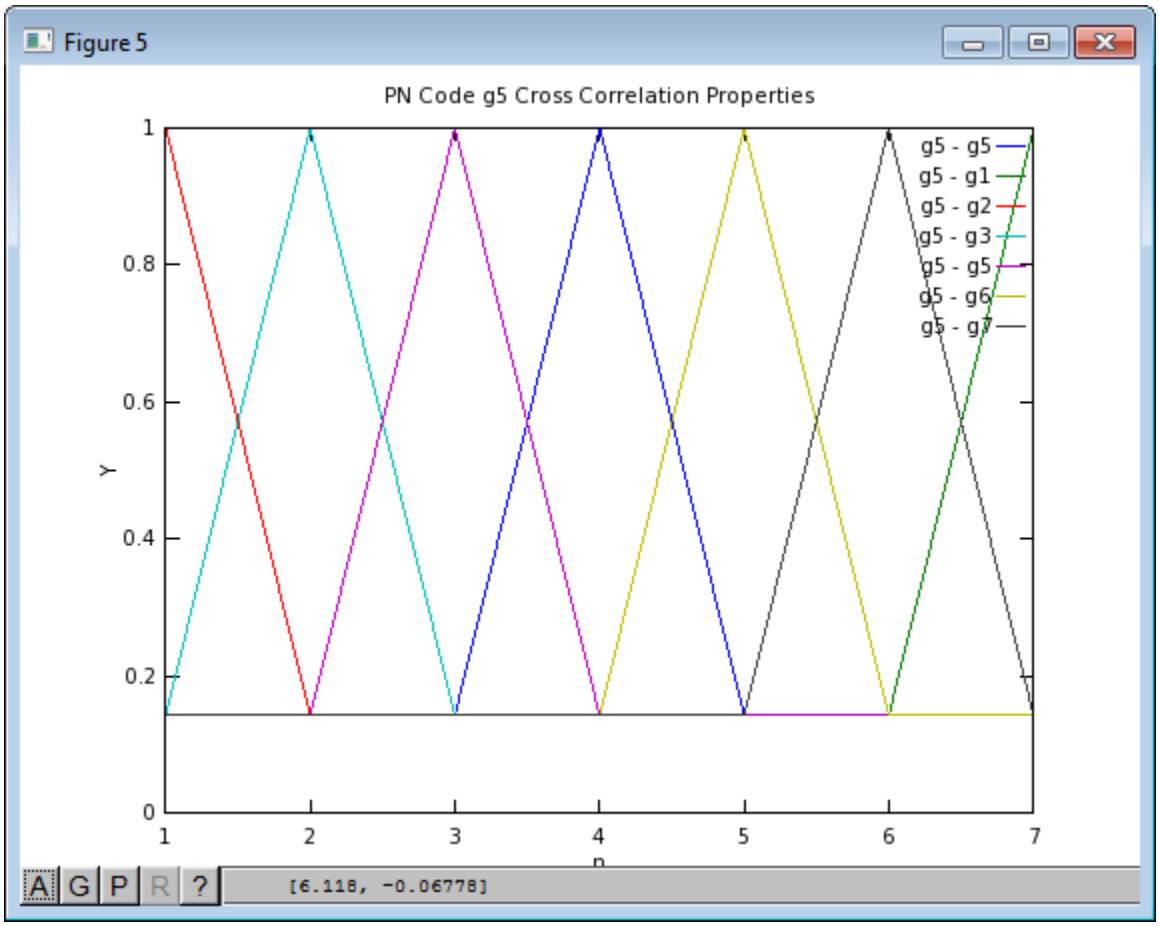

Figure 5: PN Sequence g5 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 1

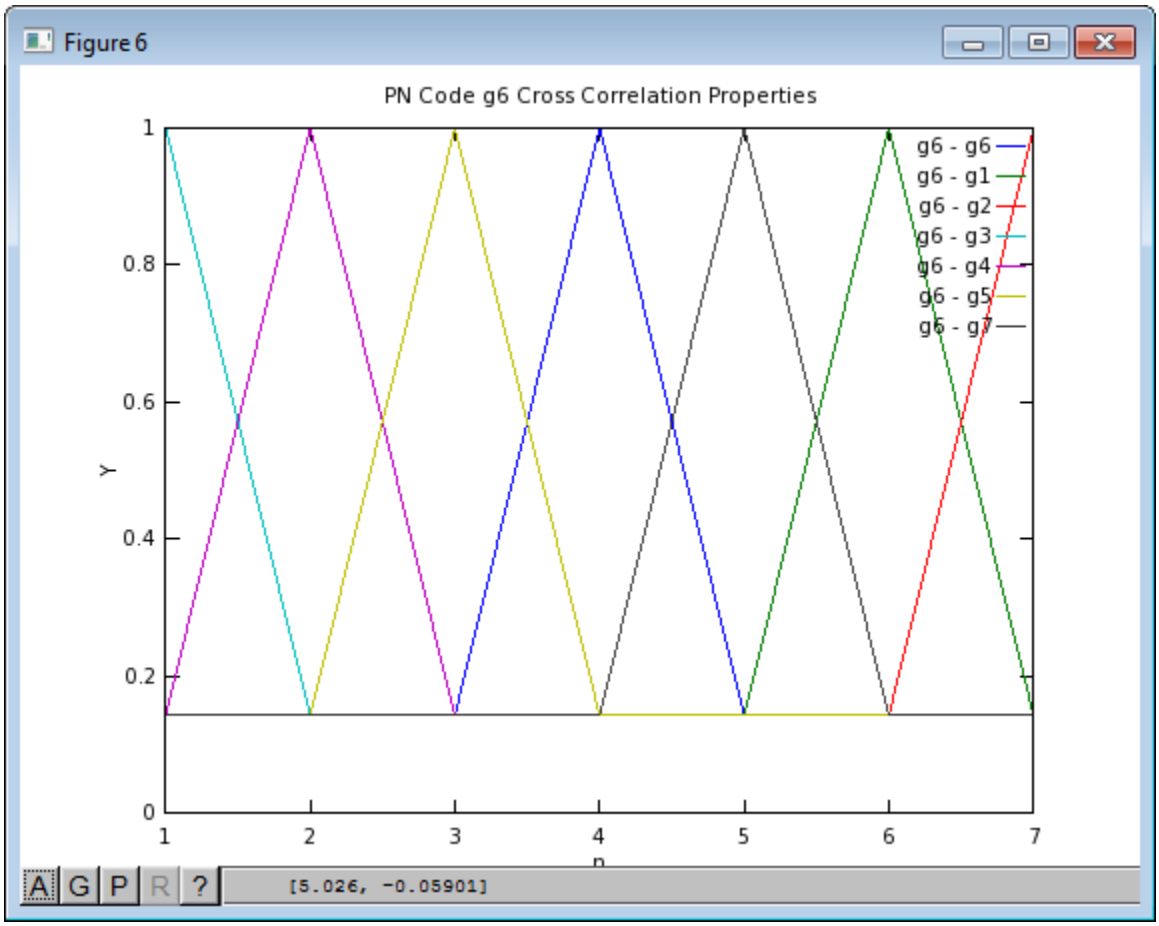

Figure 6: PN Sequence g6 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 1

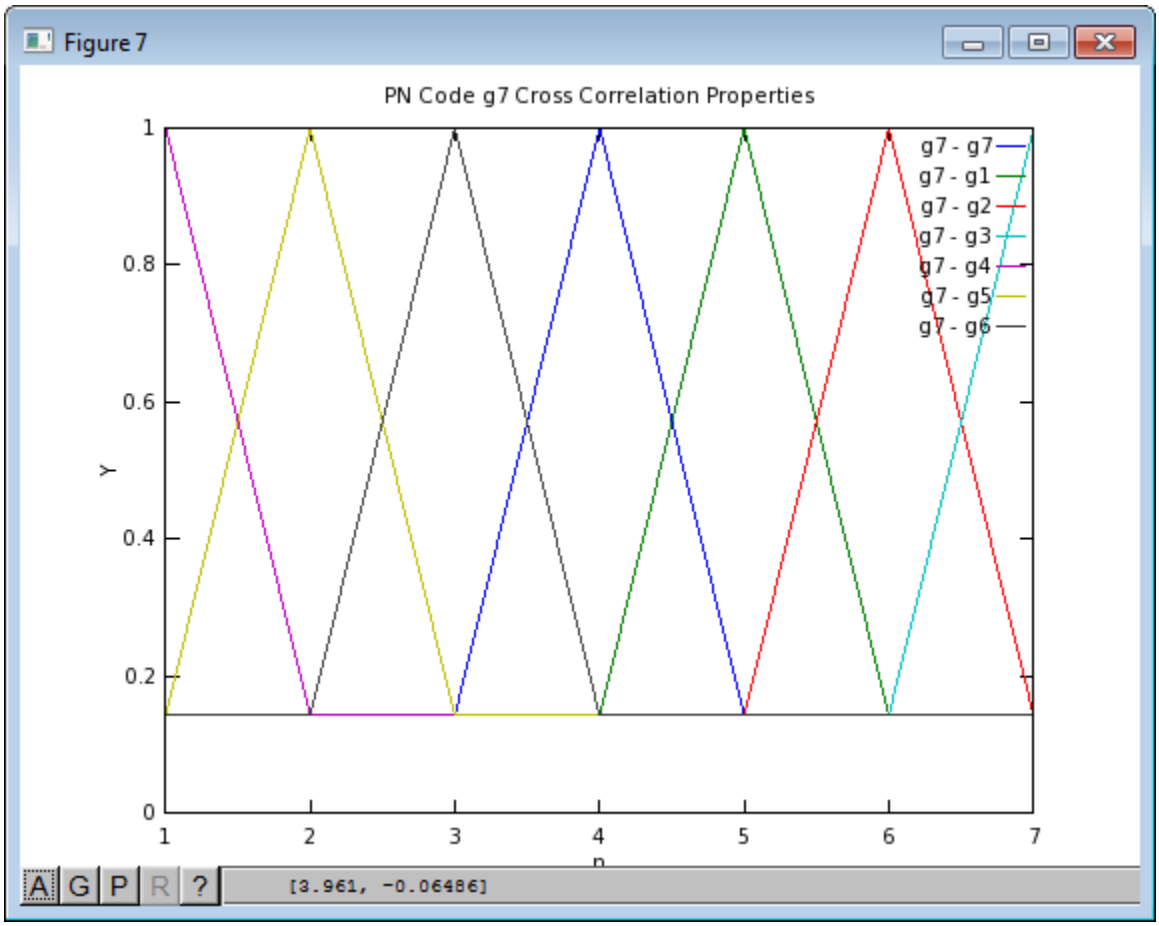

Figure 7: PN Sequence g7 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 2

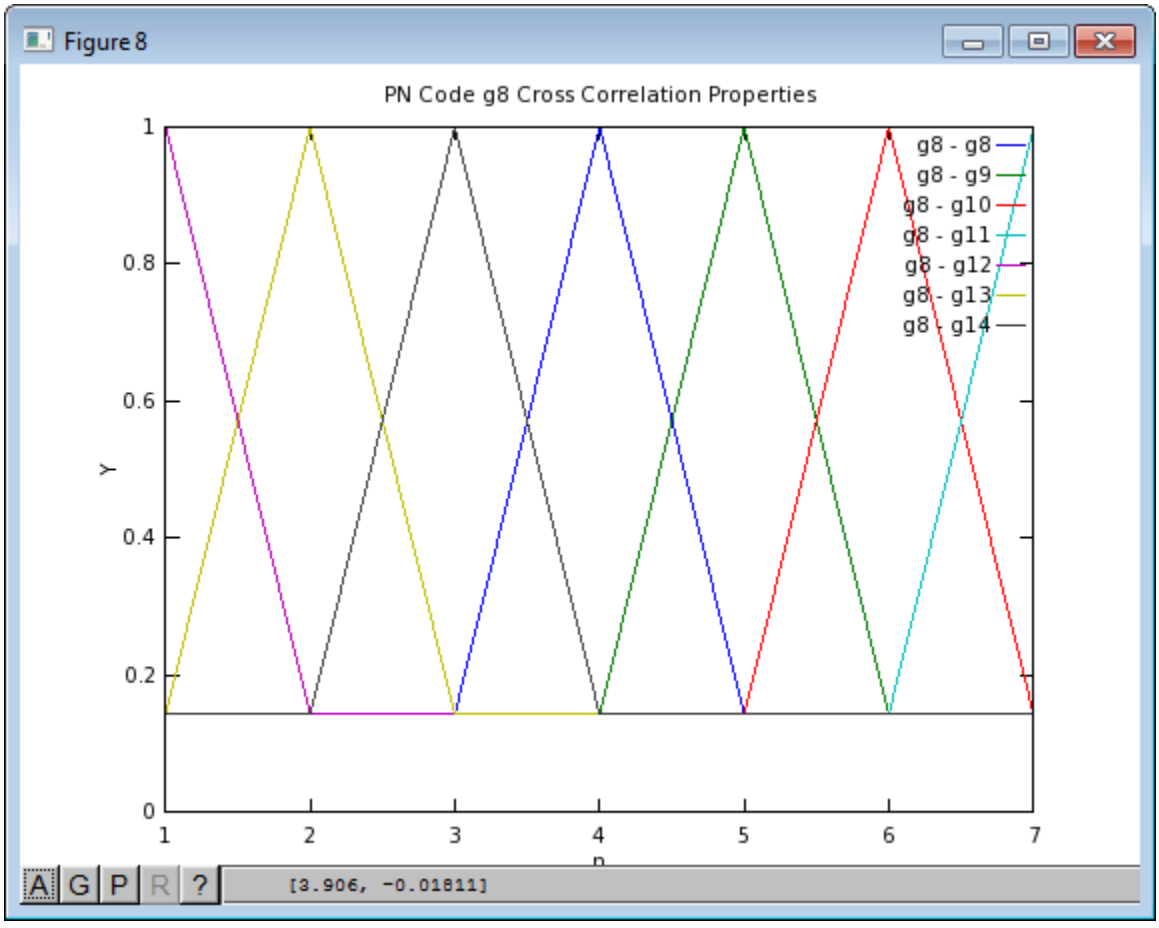

Figure 8: PN Sequence g8 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 2

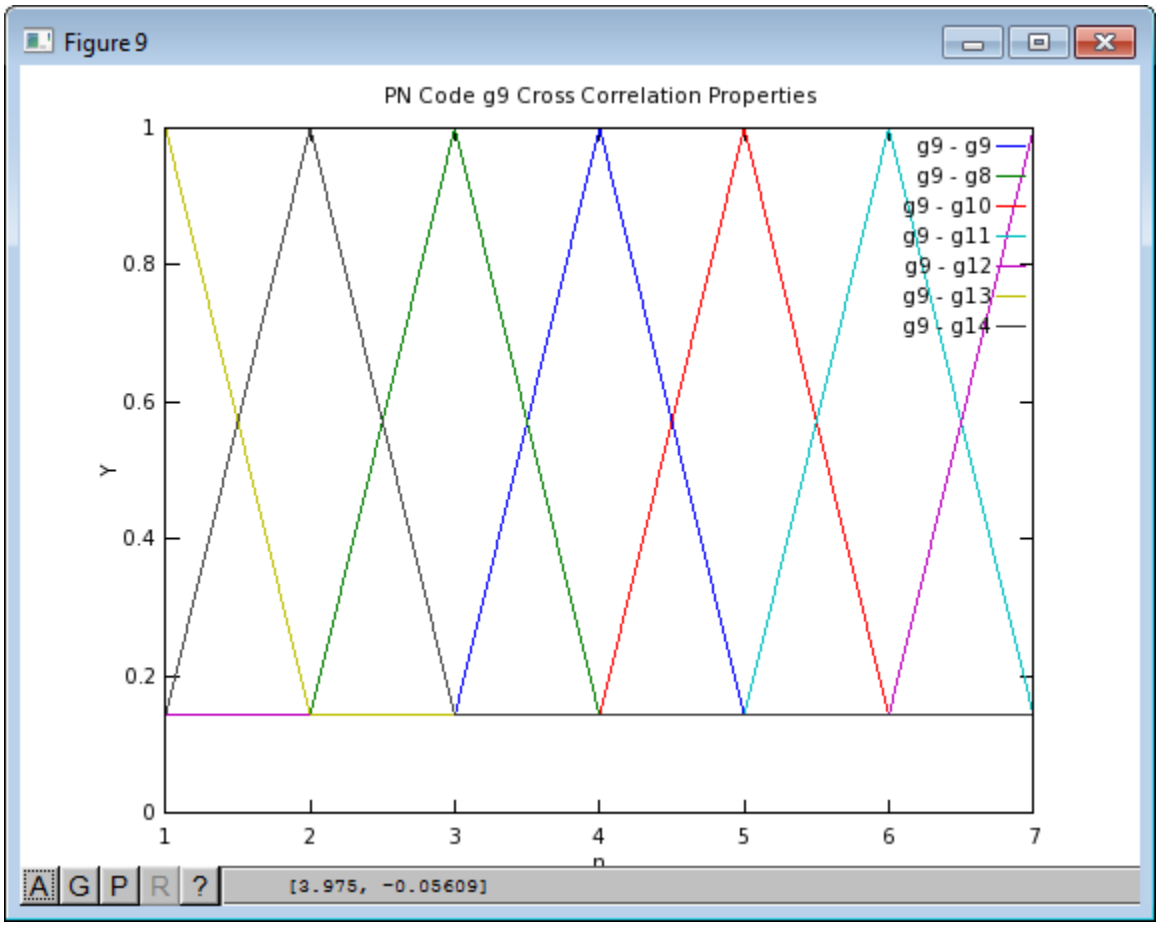

Figure 9: PN Sequence g9 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 2

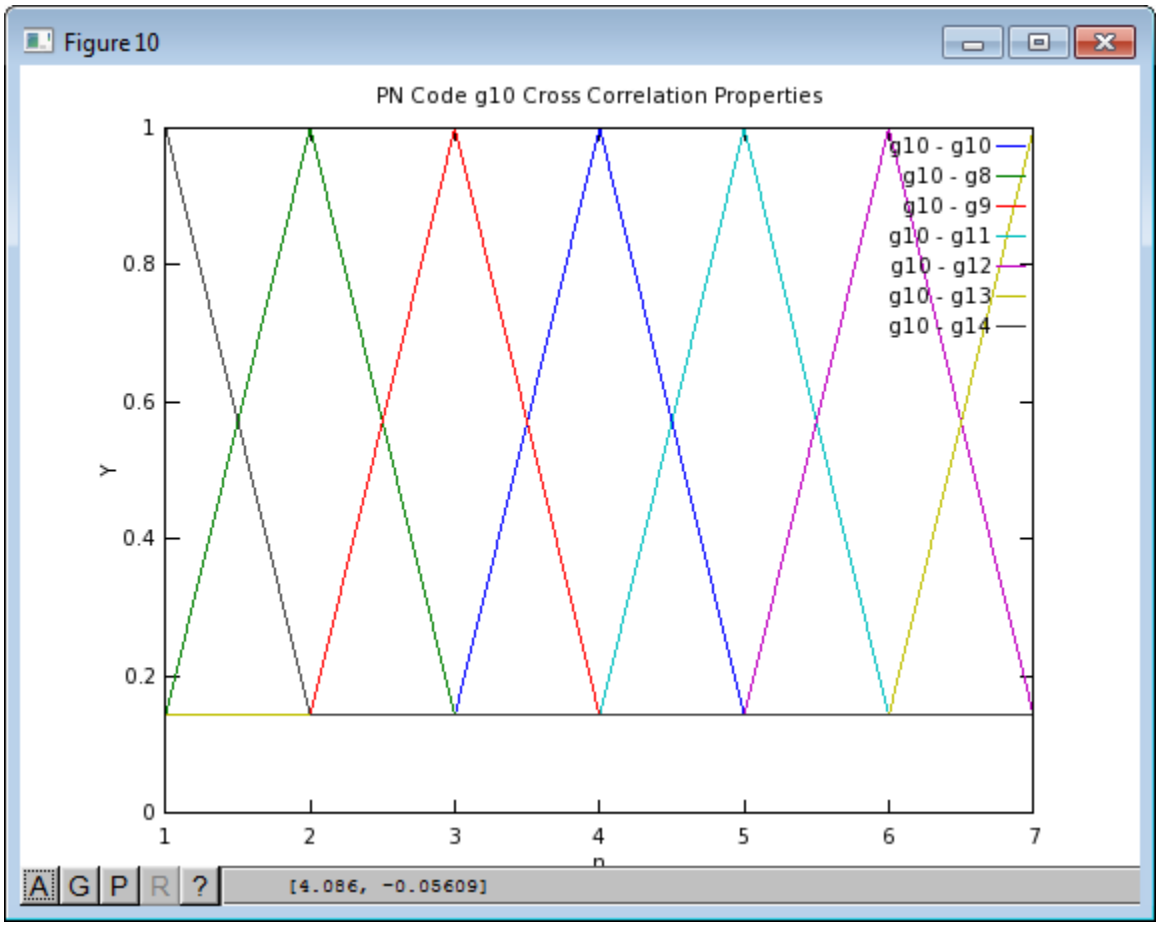

Figure 10: PN Sequence g10 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 2

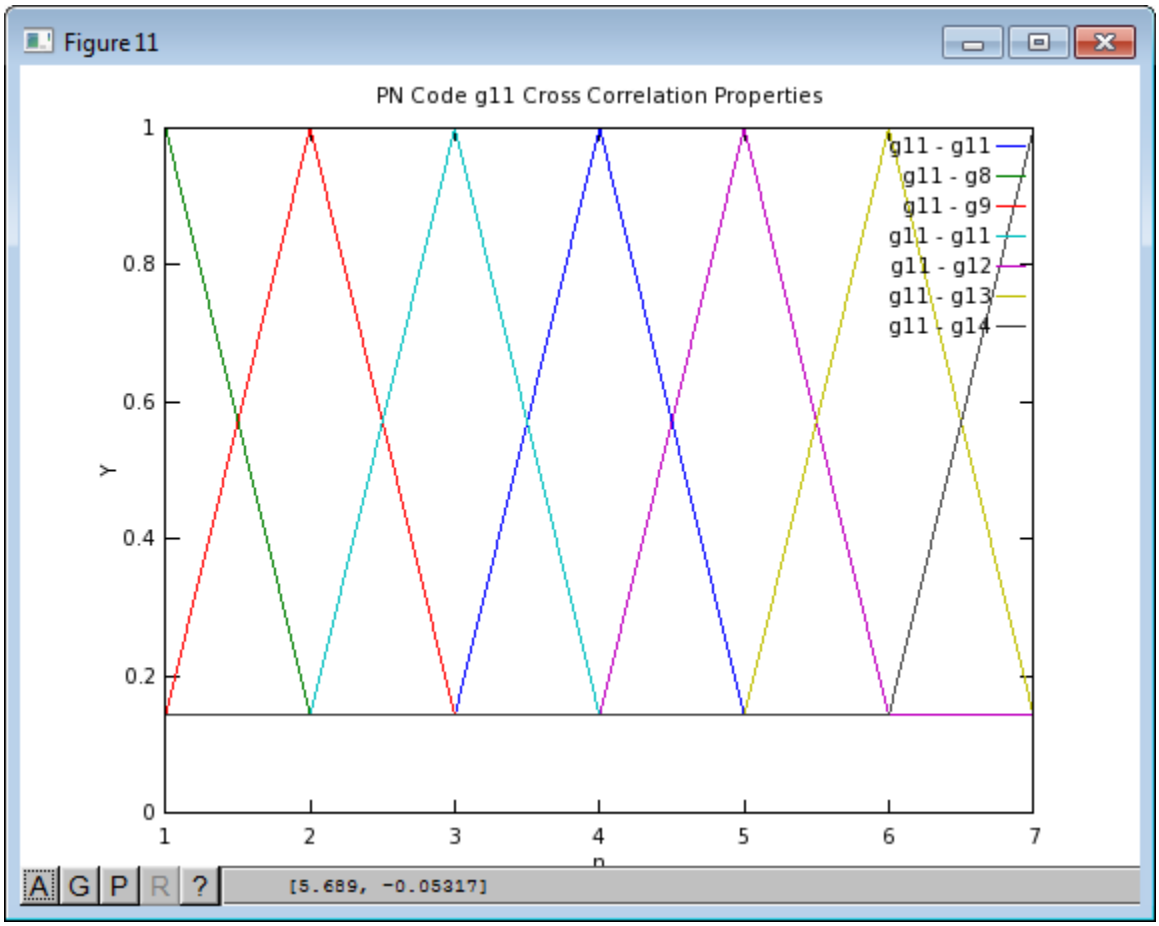

Figure 11: PN Sequence g11 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 2

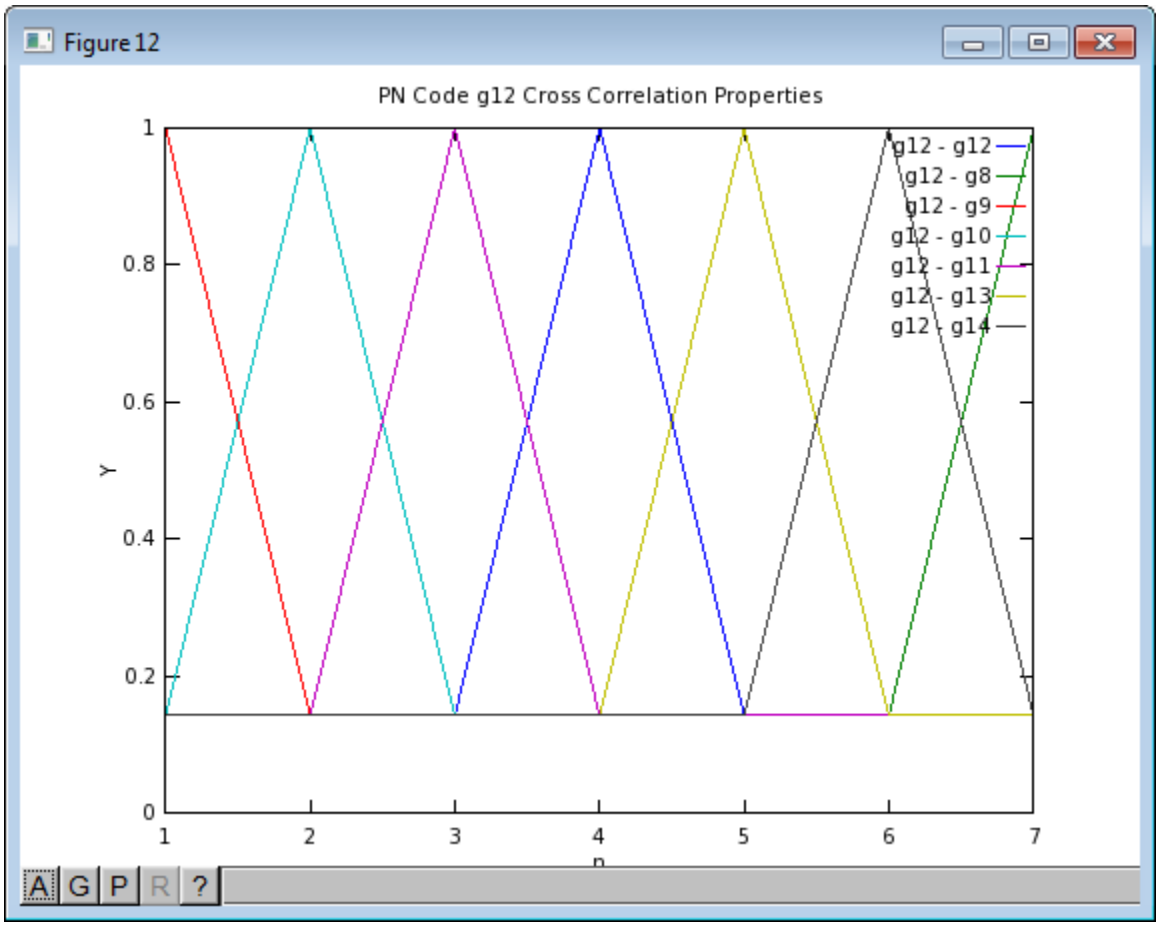

Figure 12: PN Sequence g12 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 2

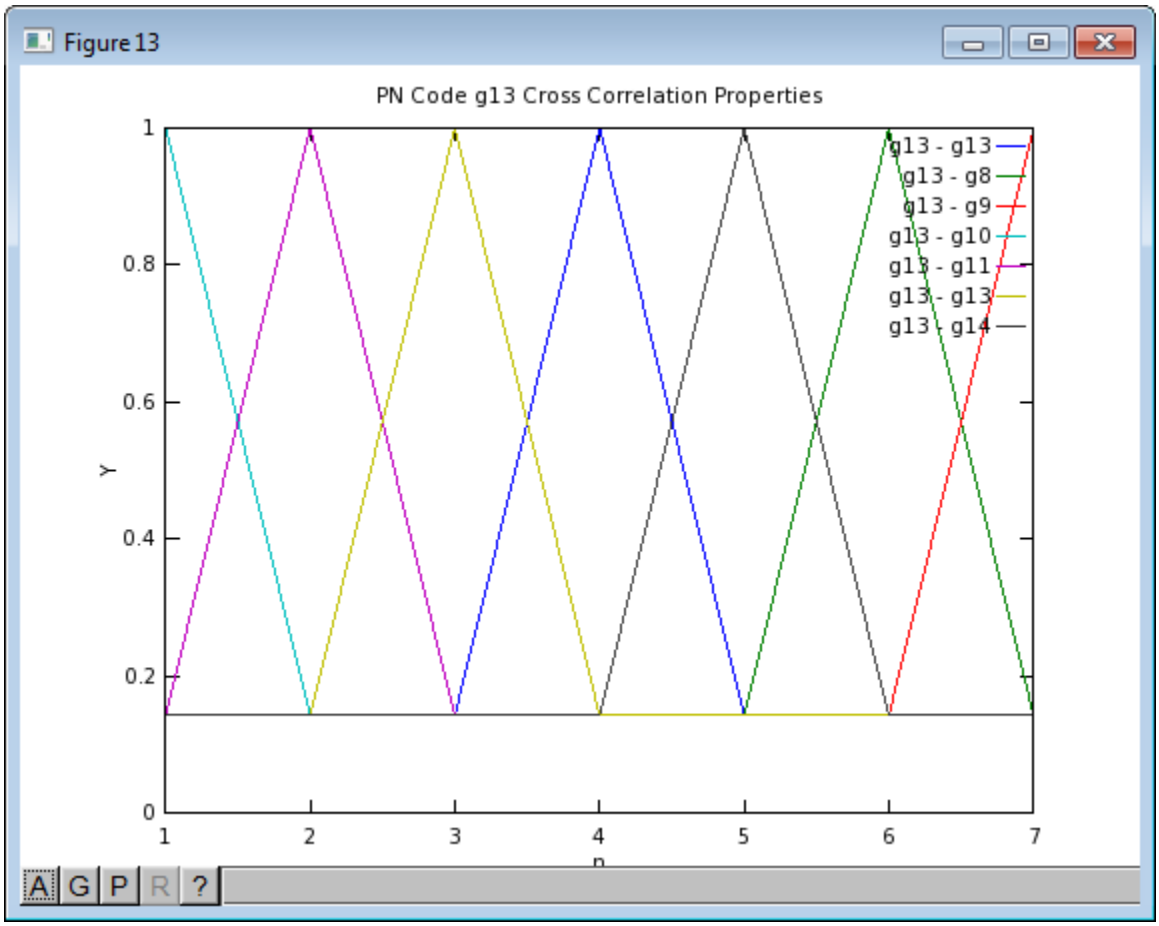

Figure 13: PN Sequence g13 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 2

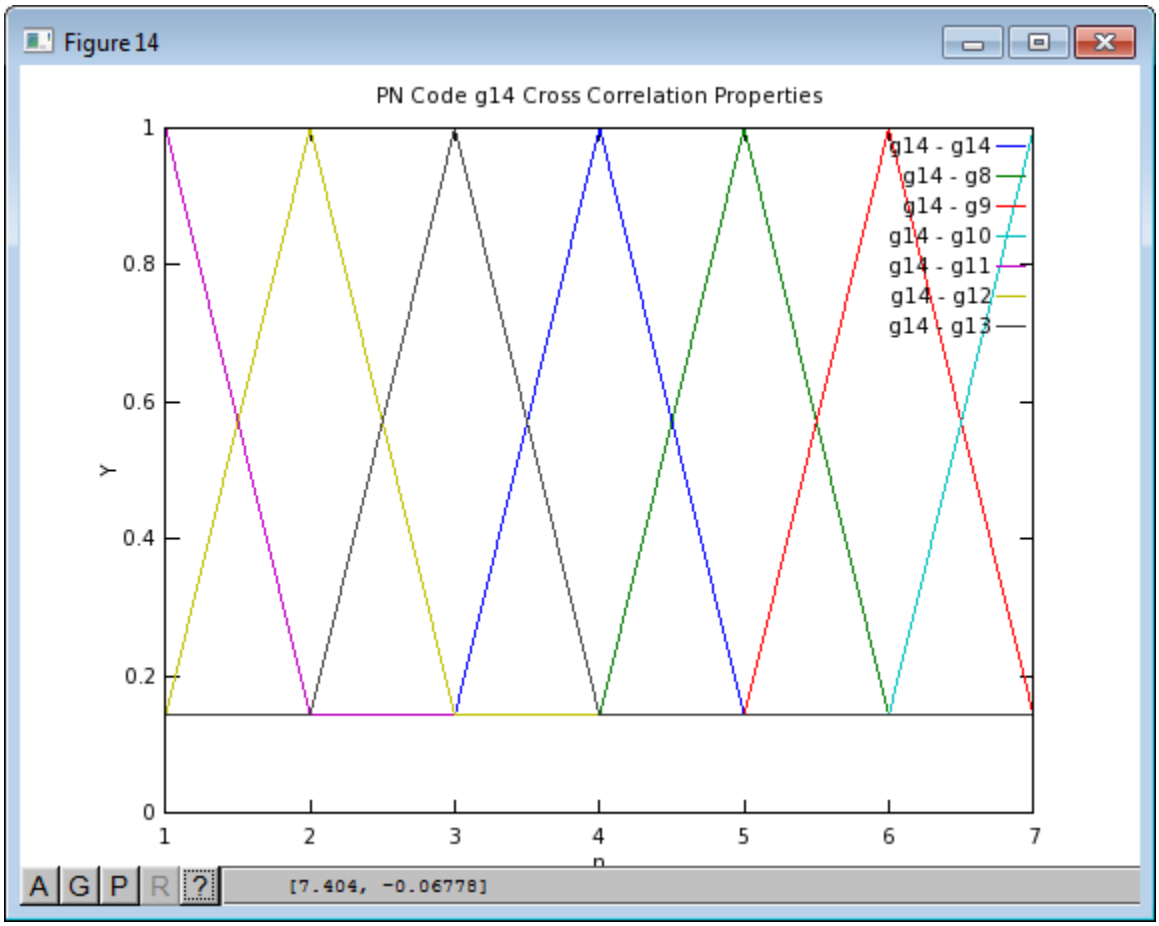

Figure 14: PN Sequence g14 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 3

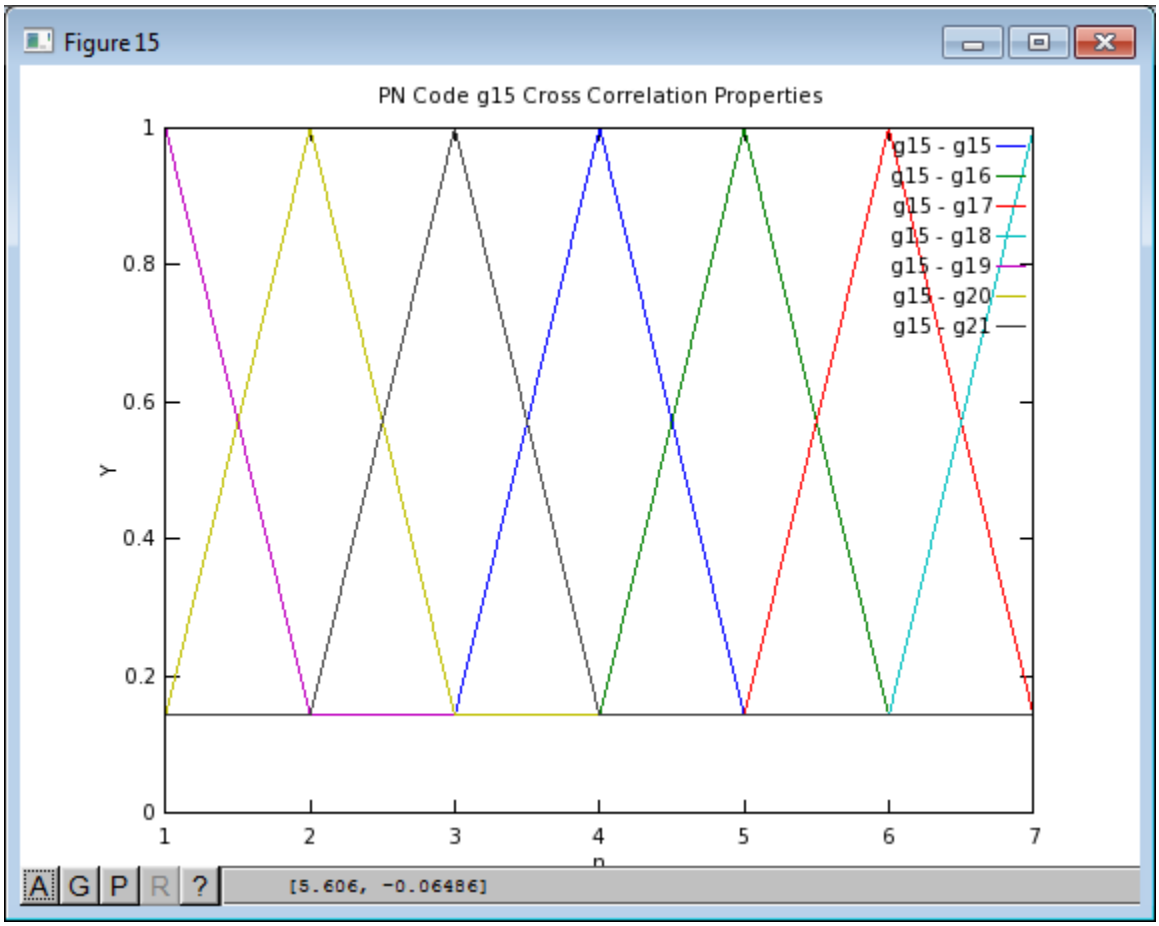

Figure 15: PN Sequence g15 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 3

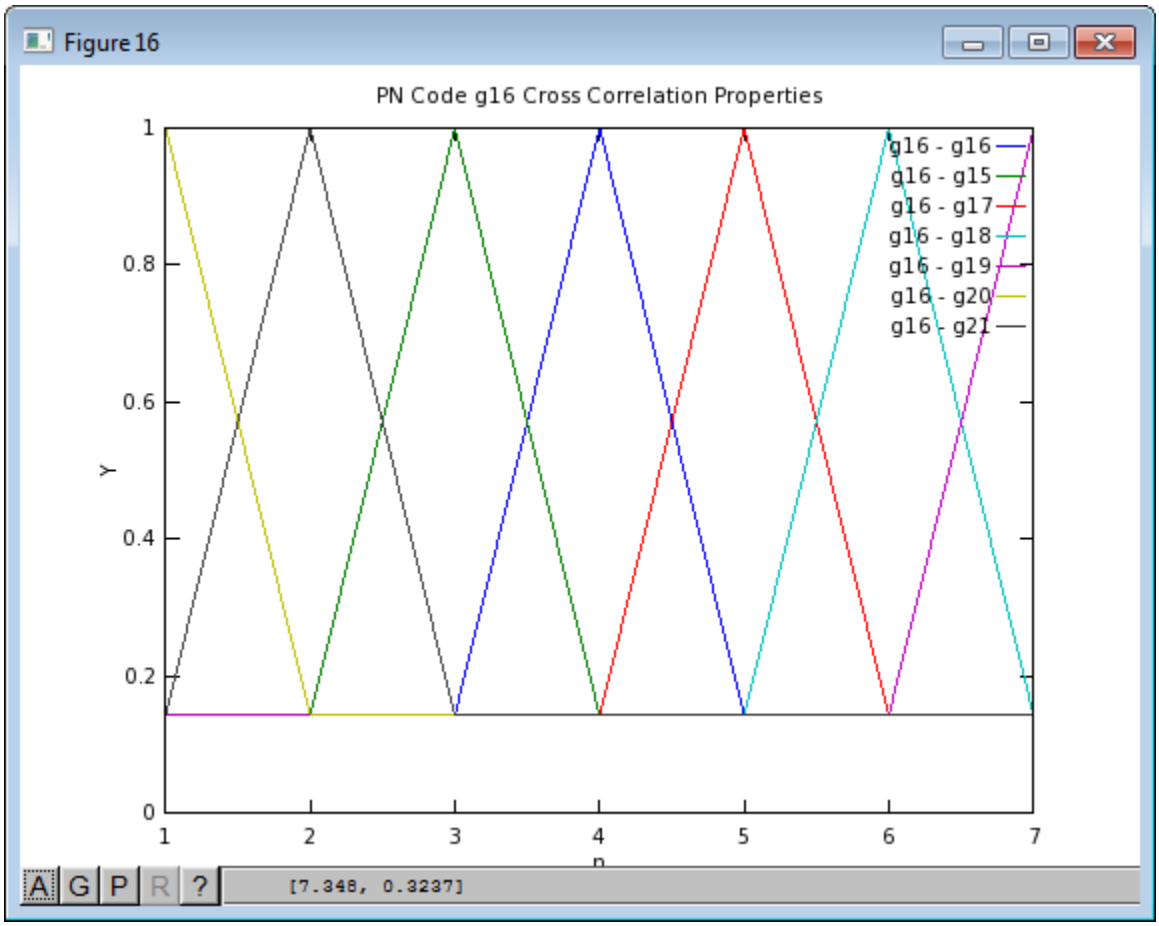

Figure 16: PN Sequence g16 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 3

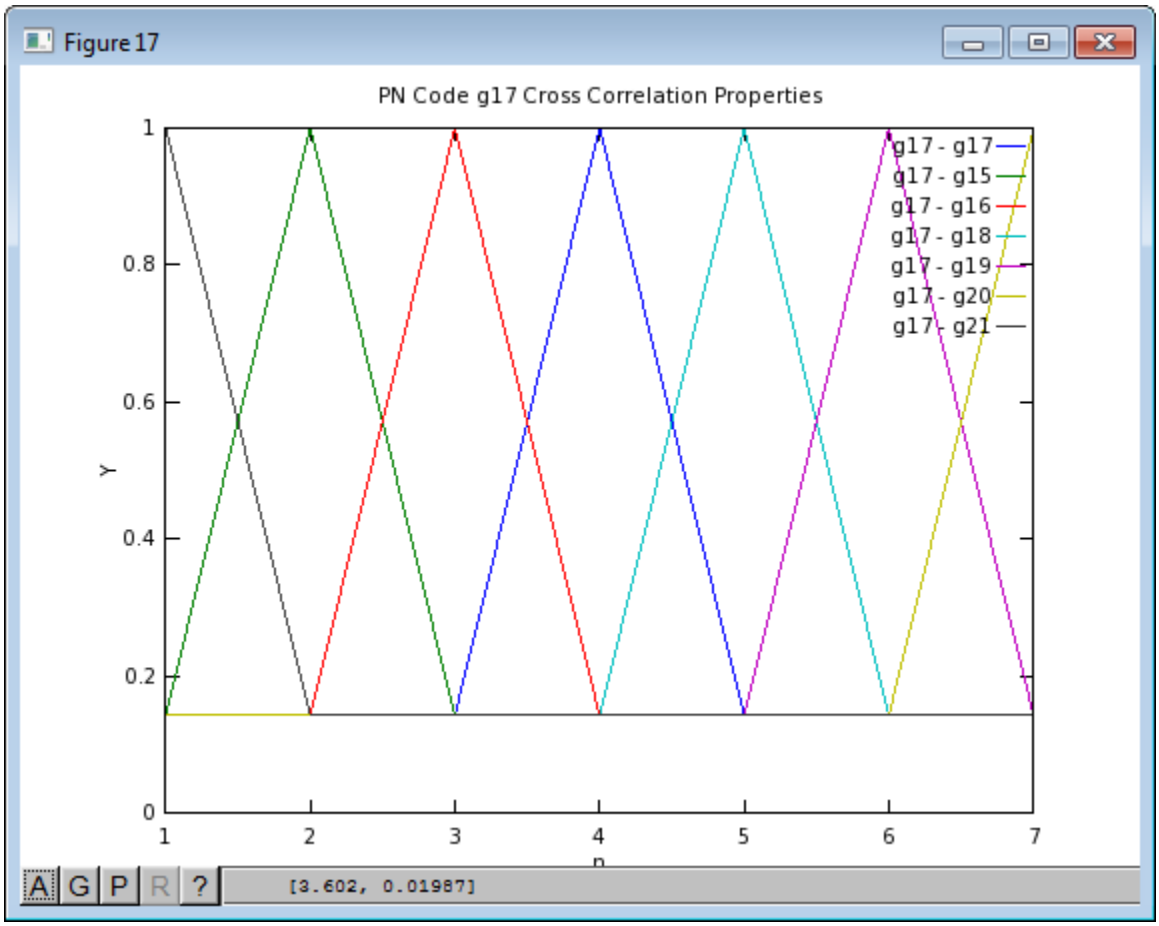

Figure 17: PN Sequence g17 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 3

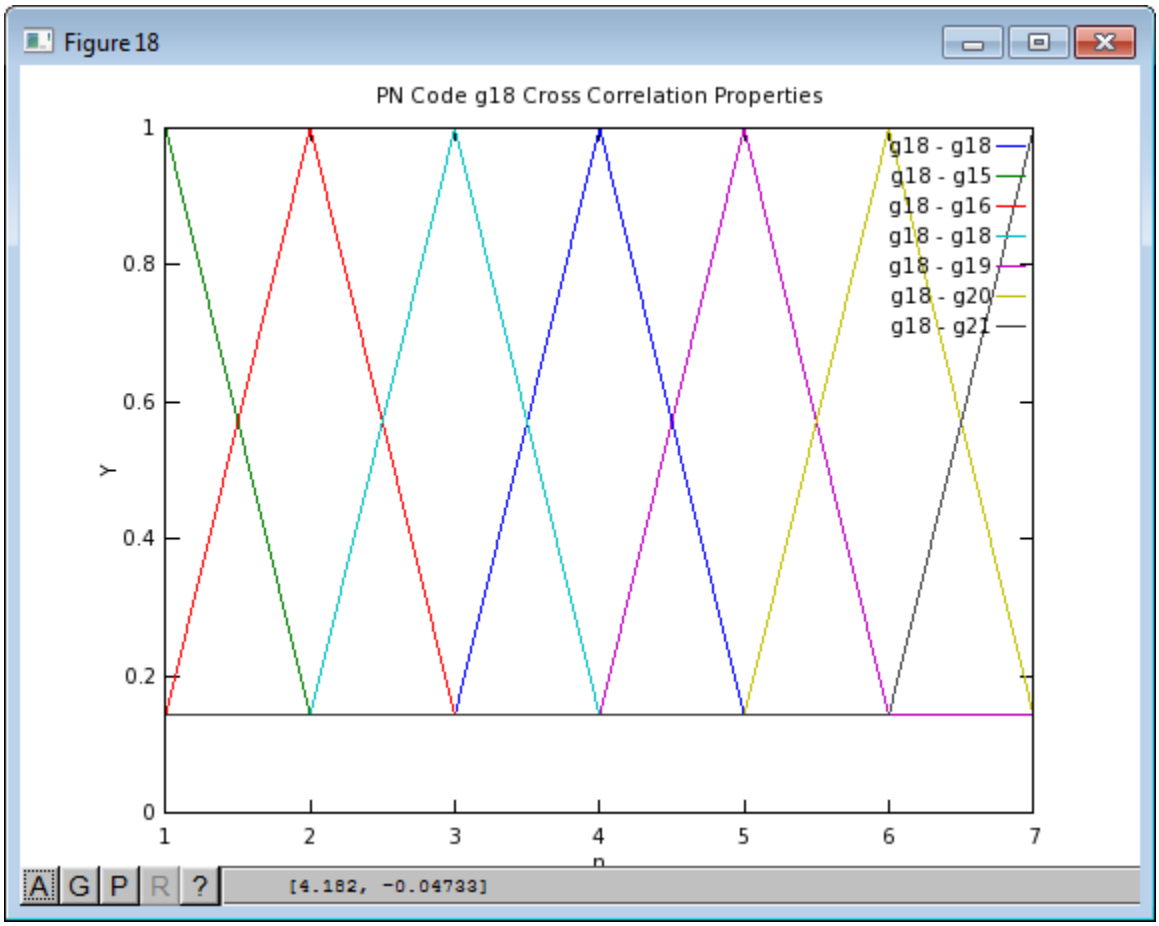

Figure 18: PN Sequence g18 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 3

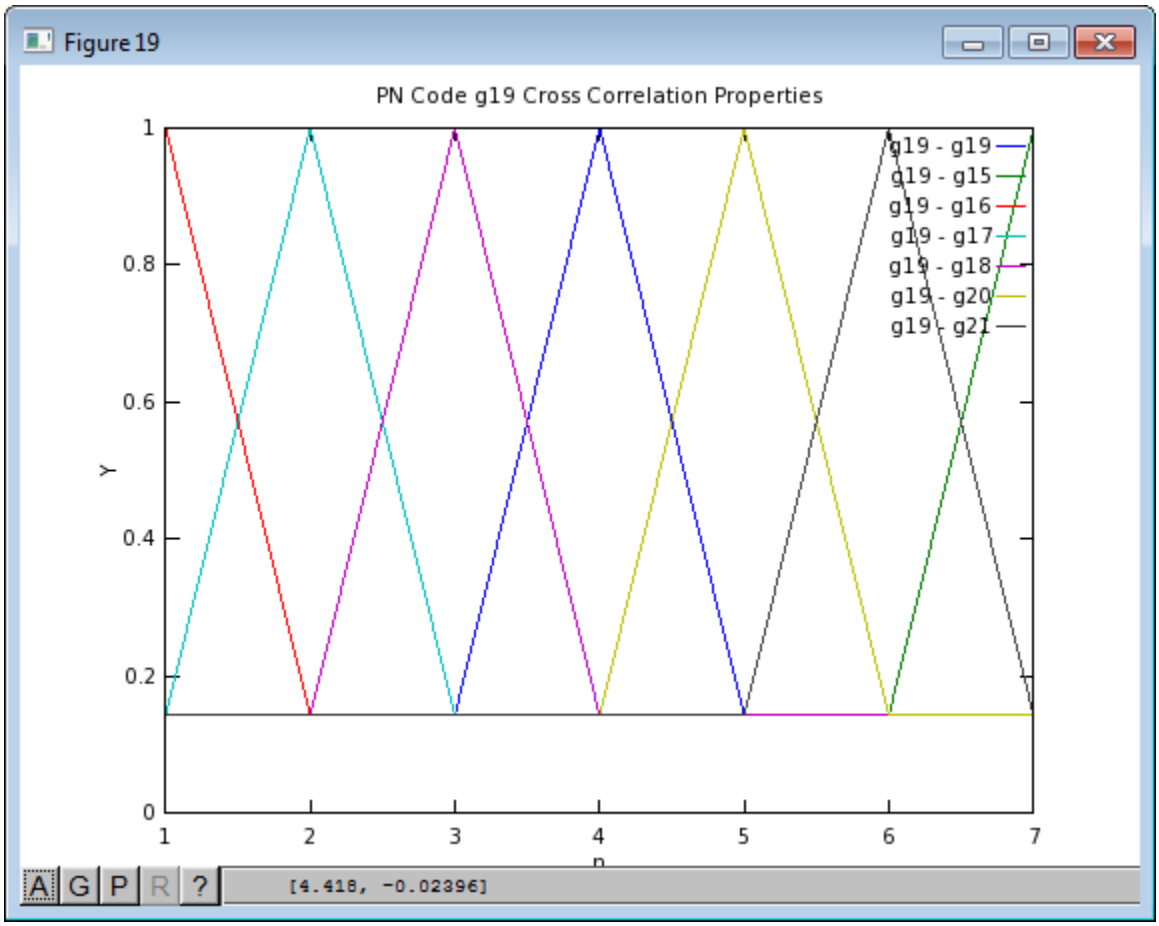

Figure 19: PN Sequence g19 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 3

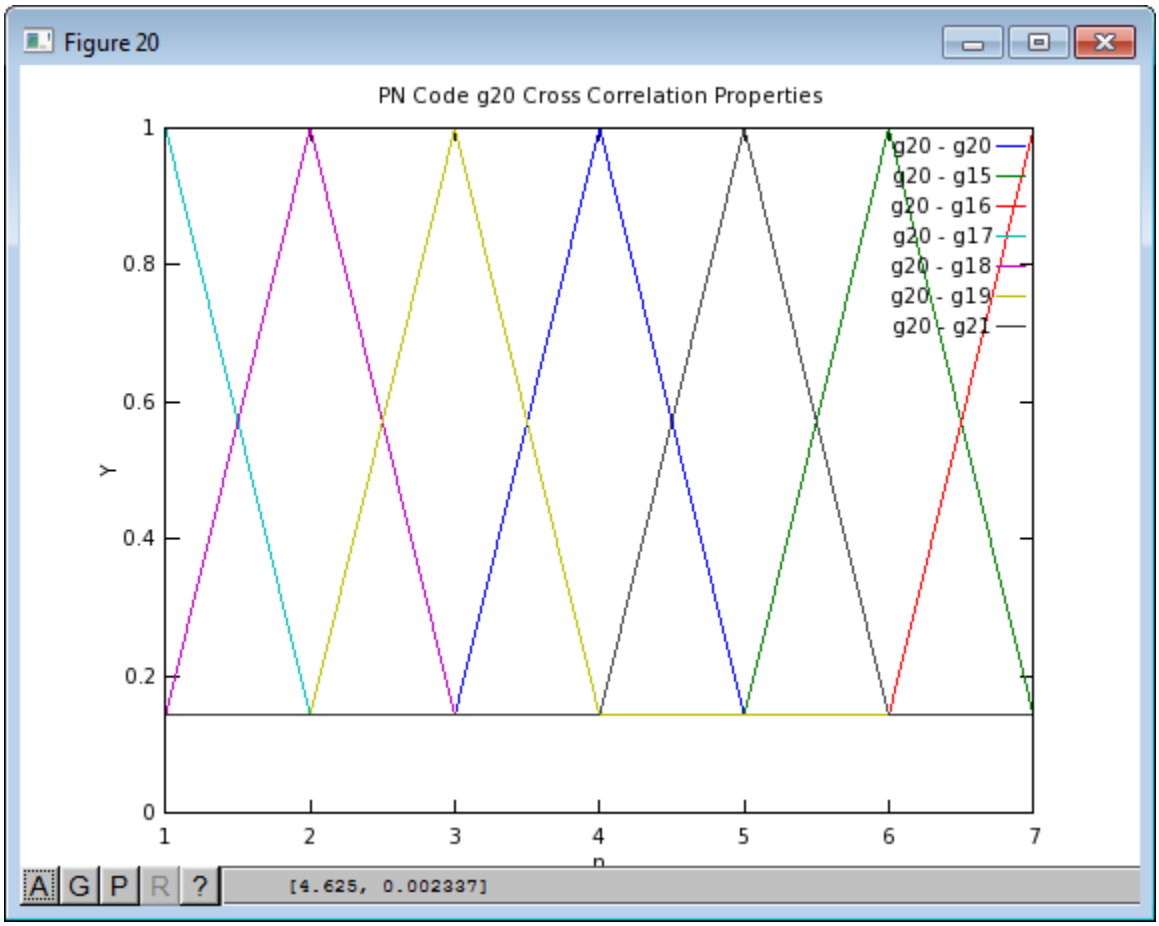

Figure 20: PN Sequence g20 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 3

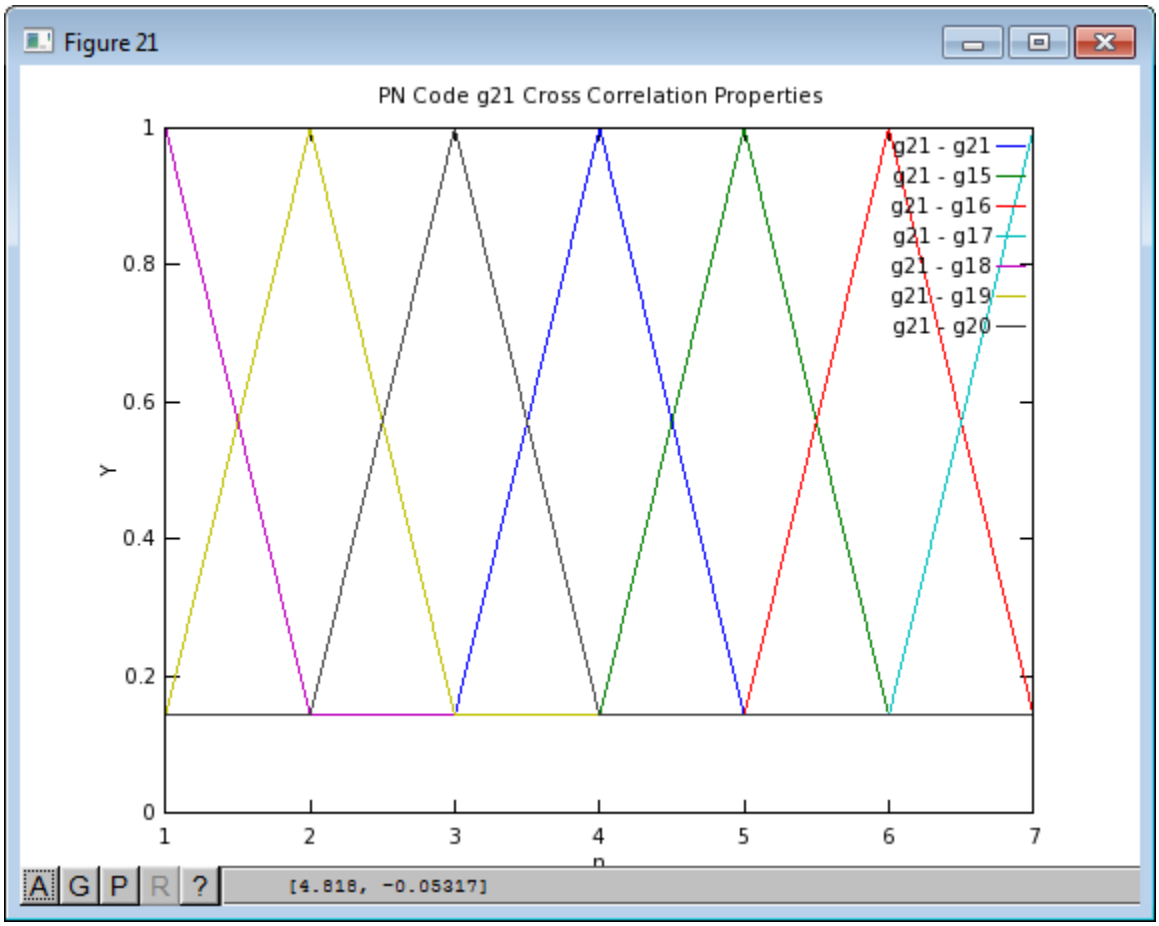

Figure 21: PN Sequence g21 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 4

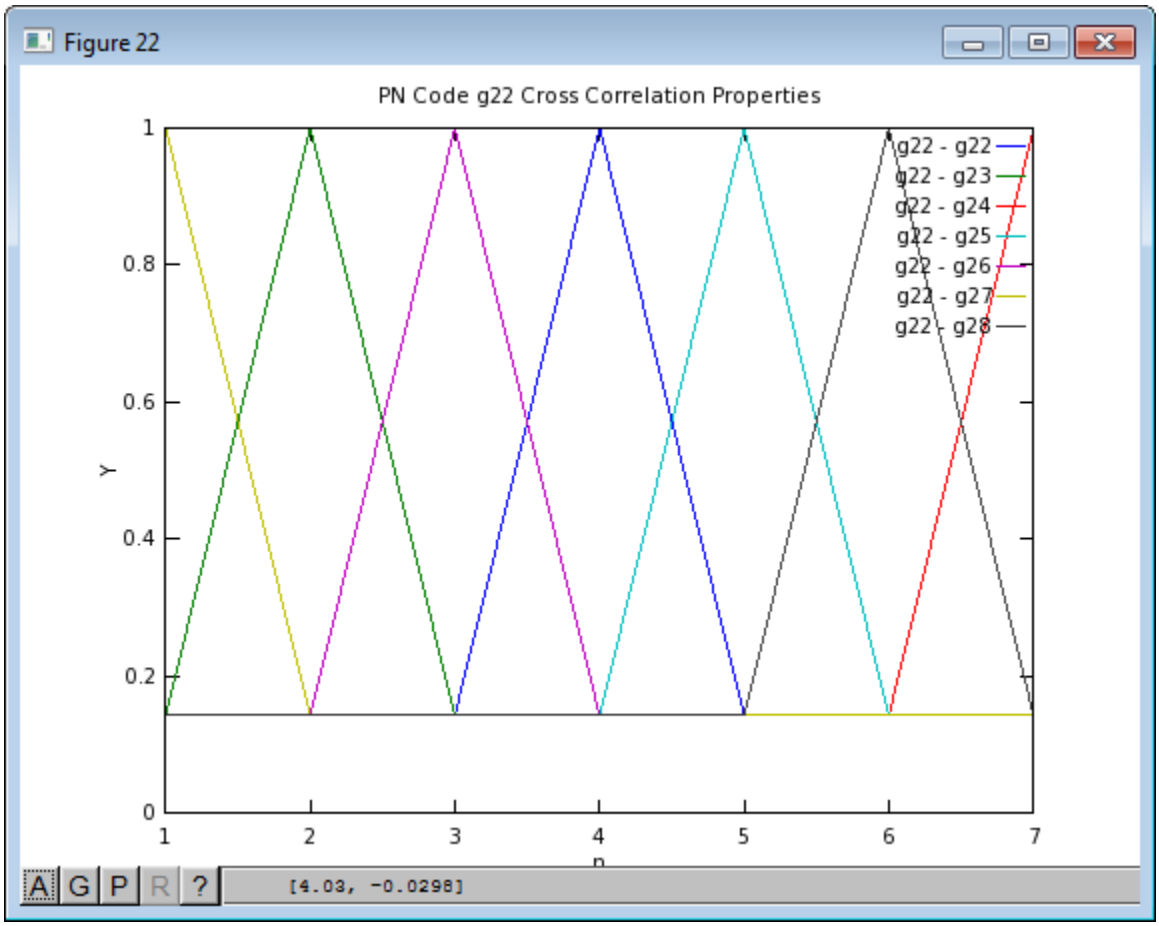

Figure 22: PN Sequence g22 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 4

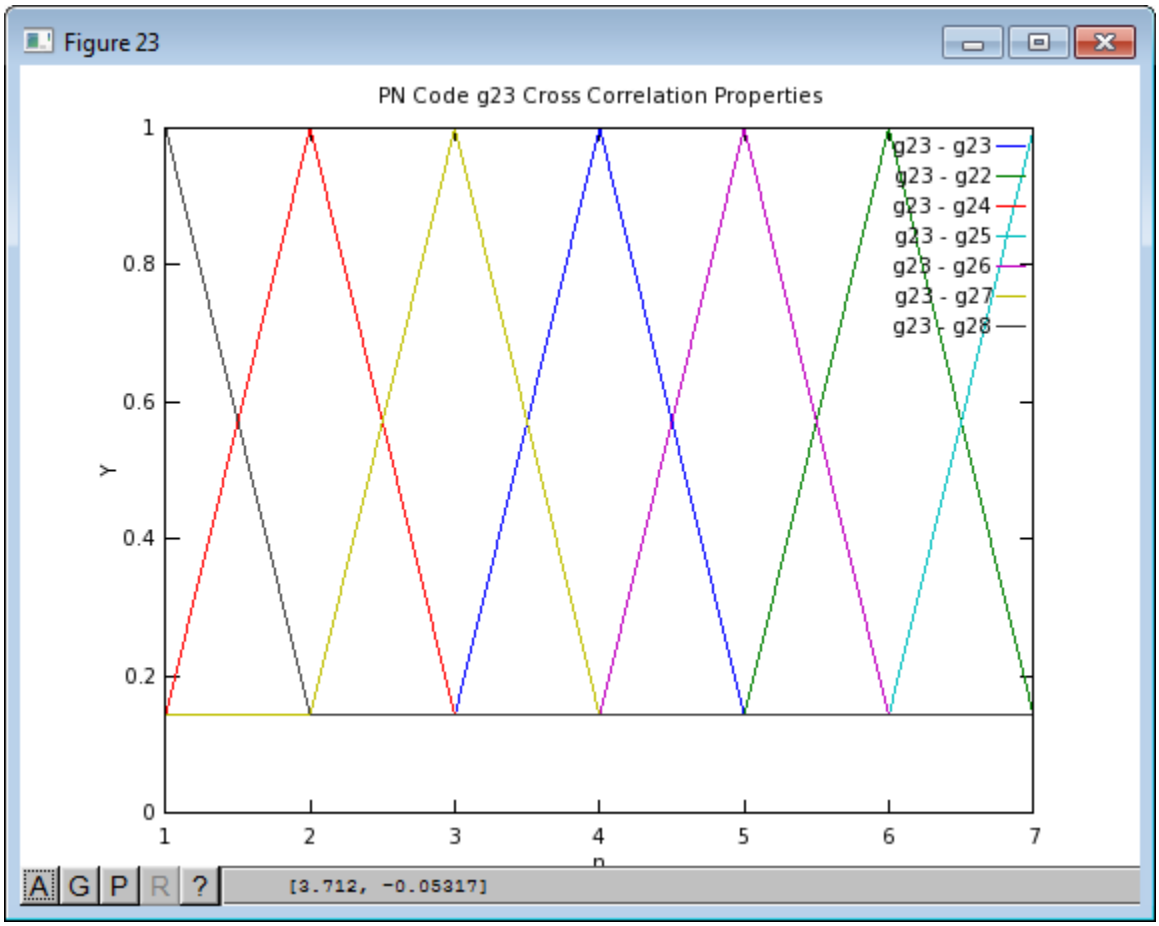

Figure 23: PN Sequence g23 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 4

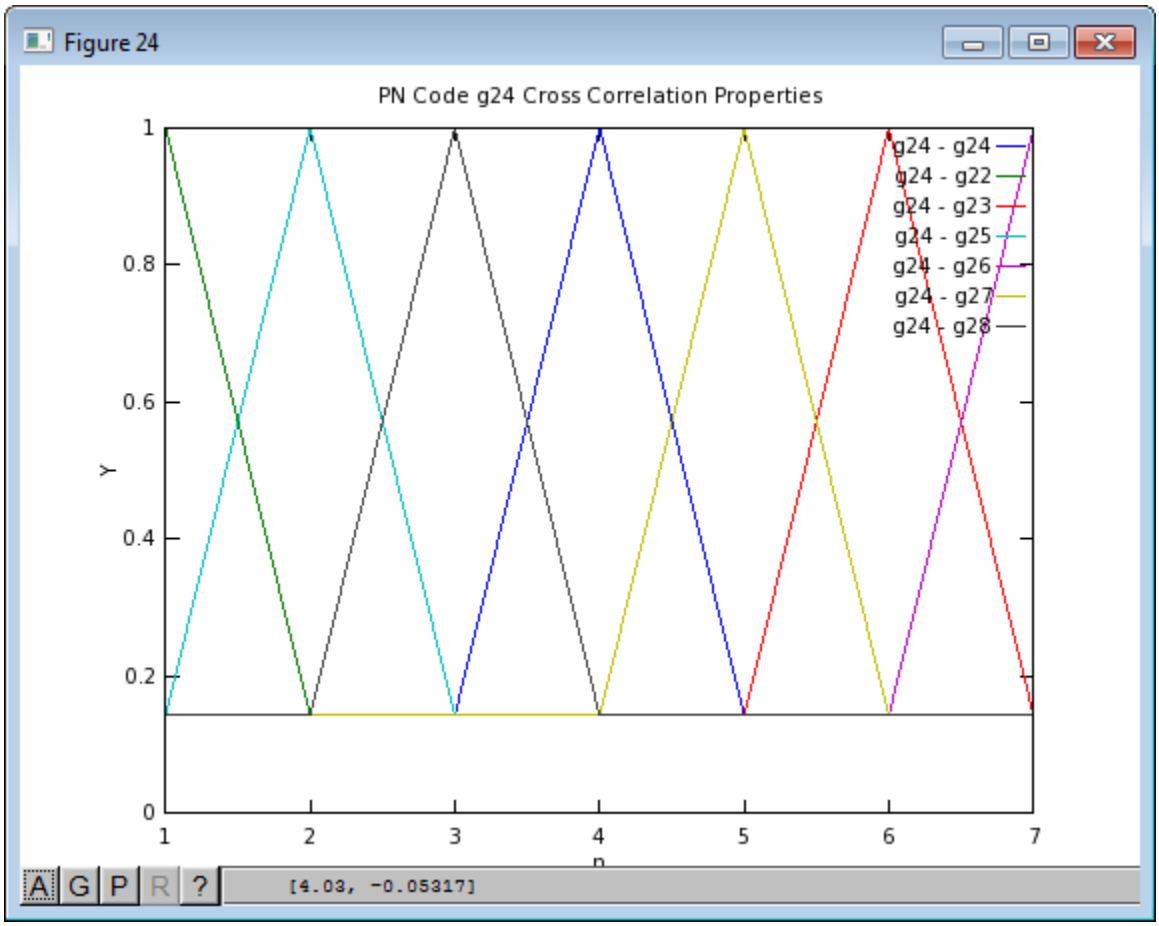

Figure 24: PN Sequence g24 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 4

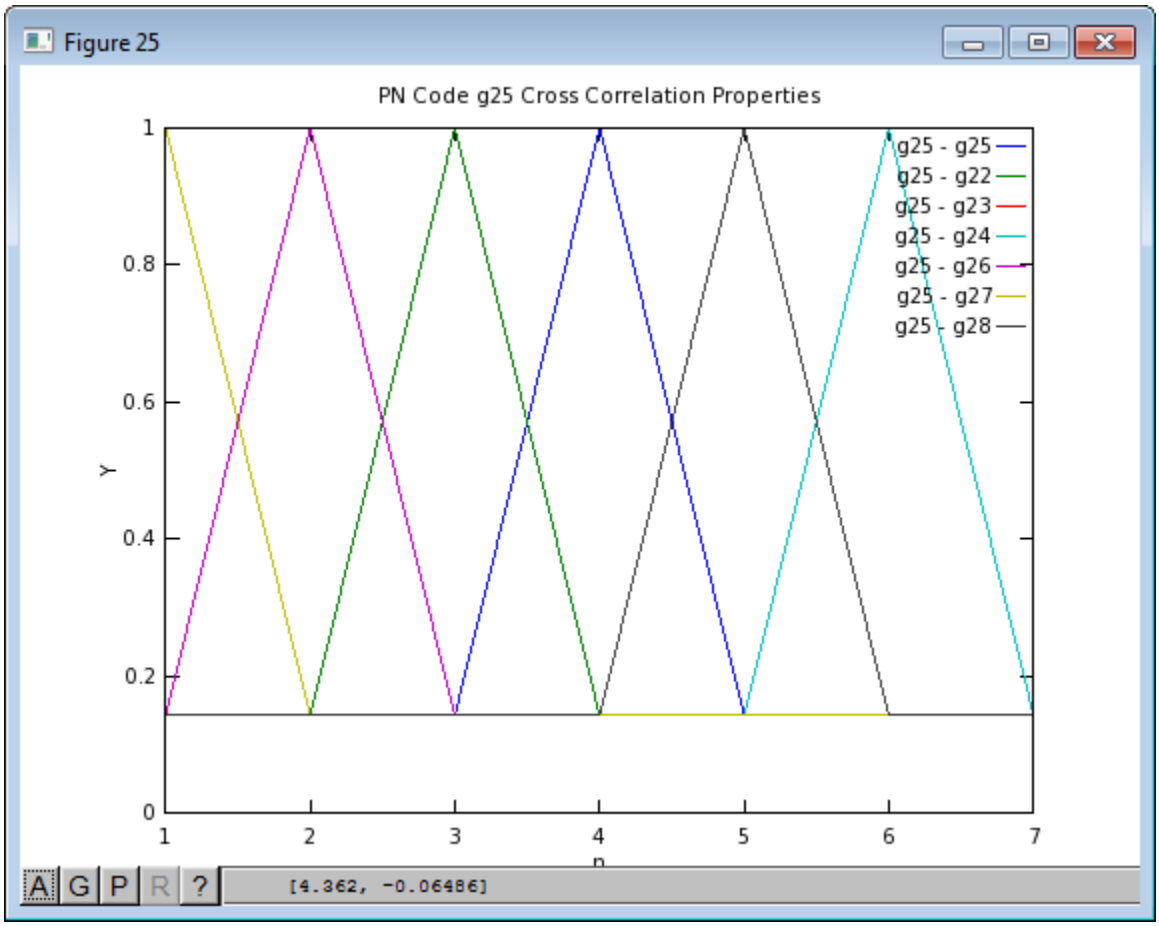

Figure 25: PN Sequence g25 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 4

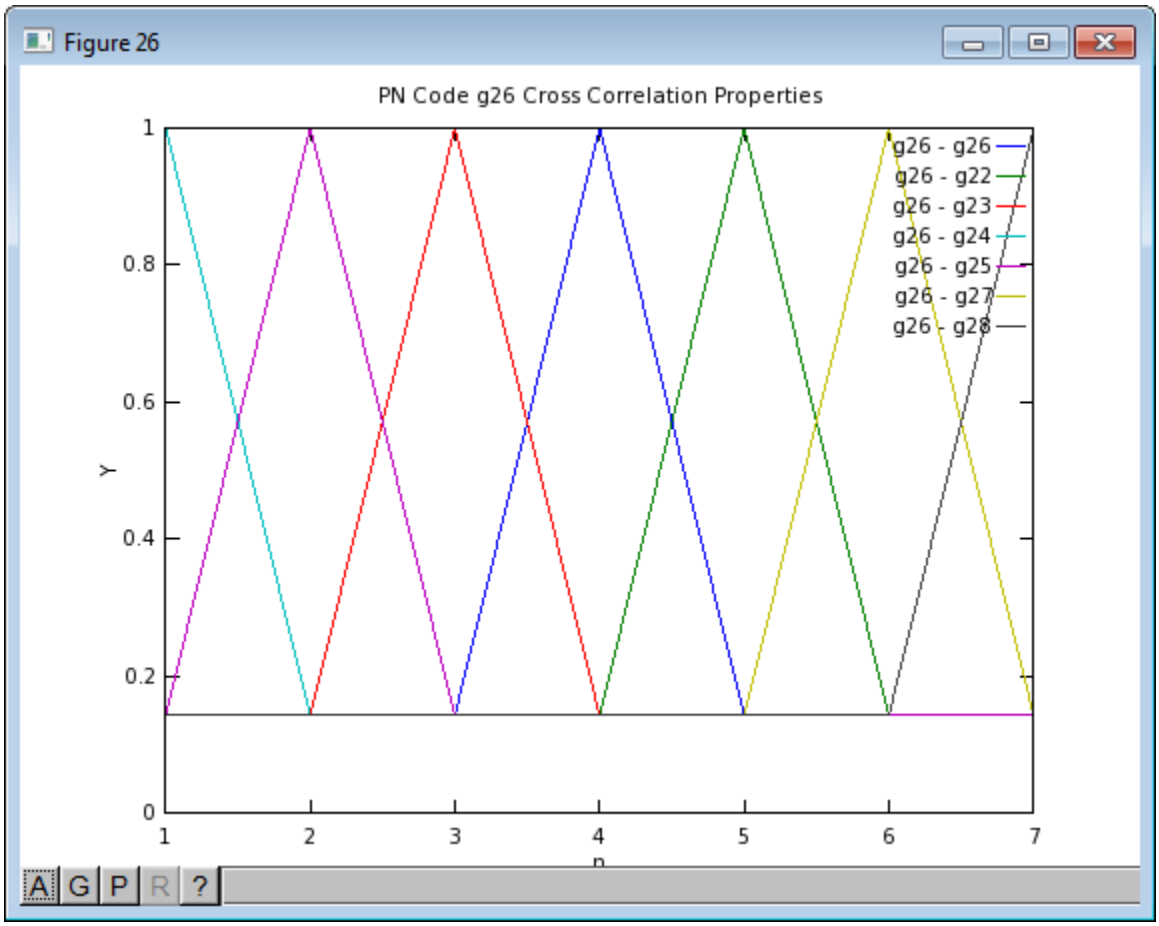

Figure 26: PN Sequence g26 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 4

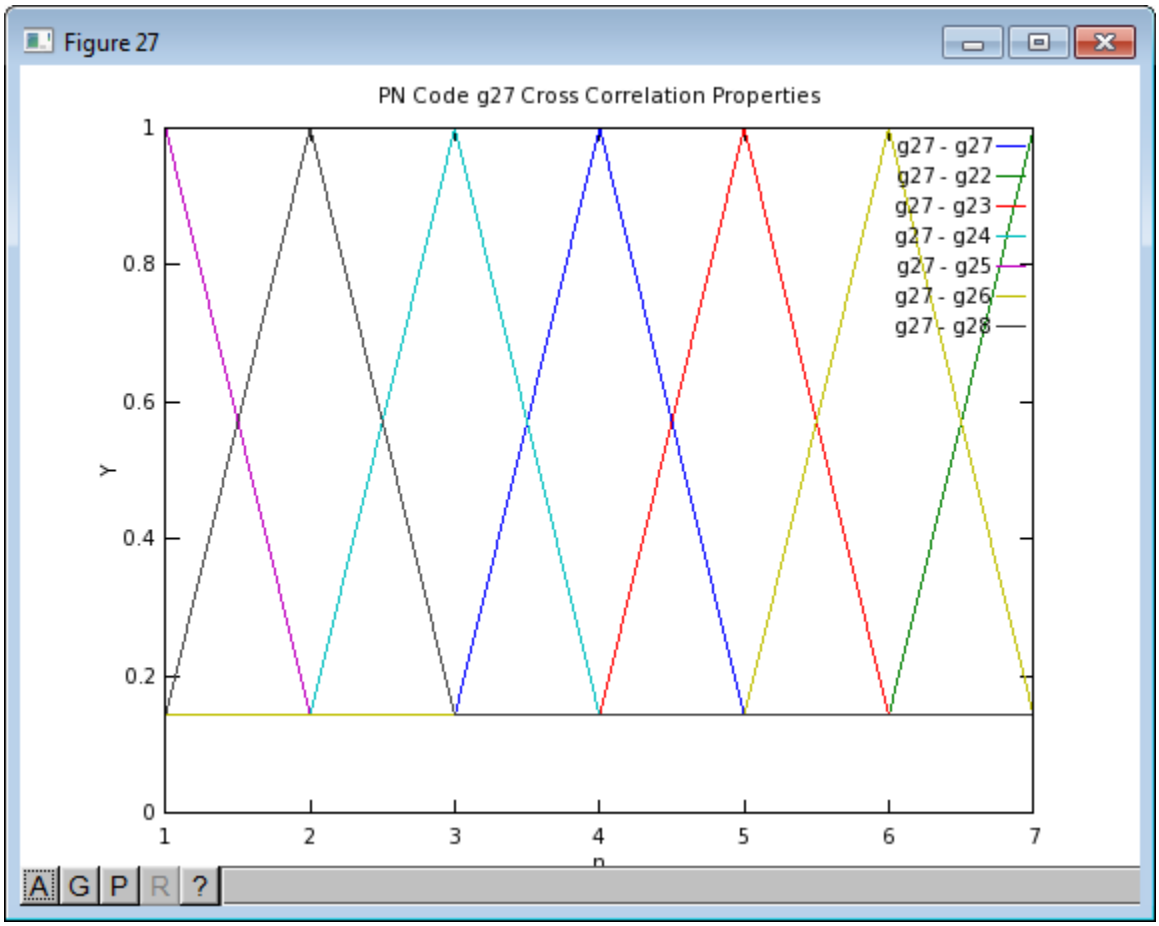

Figure 27: PN Sequence g27 Cross Correlation Properties

PN Sequence Technical Data – Cross Correlation

n = 3
Code Length = 7
28 Codes (PN1 – PN28)
4 Groups - 7 Codes / Group

Group 4

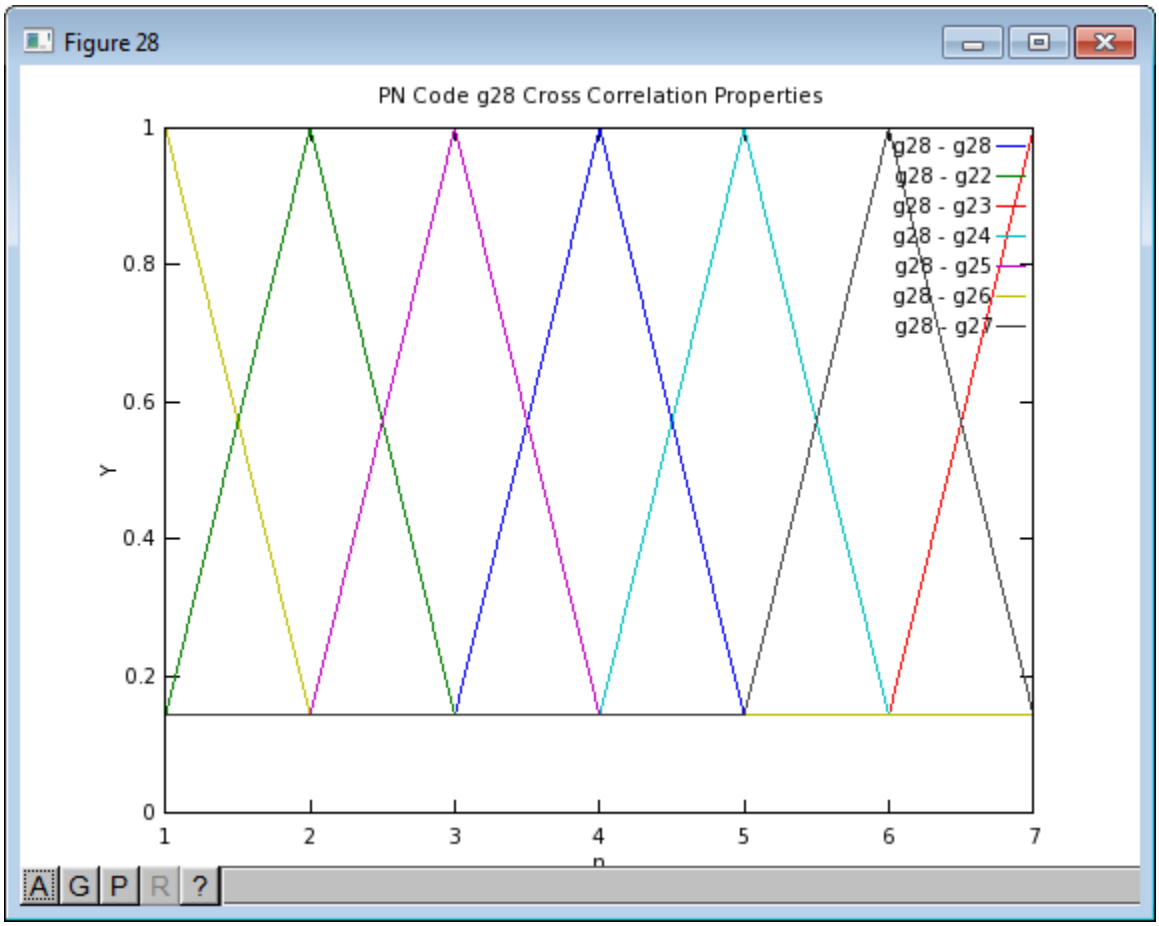

Figure 28: PN Sequence g28 Cross Correlation Properties

Aurelii Communications

Preliminary Data Sheet

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