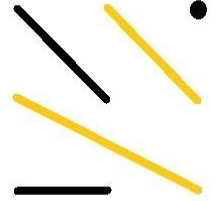




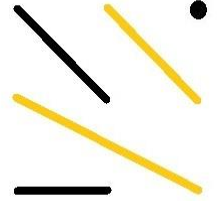
Customer Presentation

Agenda



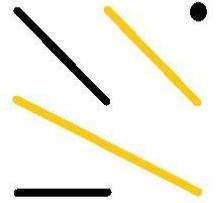
- Mission Statement
- Product Offering
- Product Examples
- Timeline

Legal Statement



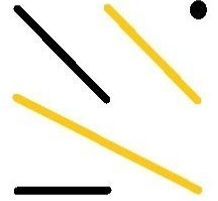
- All designs contained herein are protected under United States Patent/Copyright/Trademark/Trade Secret/Unfair Competition Laws

Mission Statement



To provide the very best communication solutions to customers requiring secure communication technologies for transmission over mainstream or evolving networks.

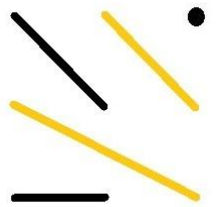
Product Offering



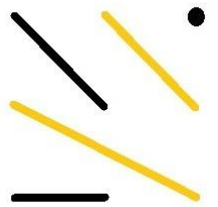
Semiconductor Intellectual Property

- Gold Code Generators
- Auto-Correlation
- Cross-Correlation

Product Offering



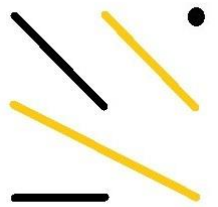
Gold Codes



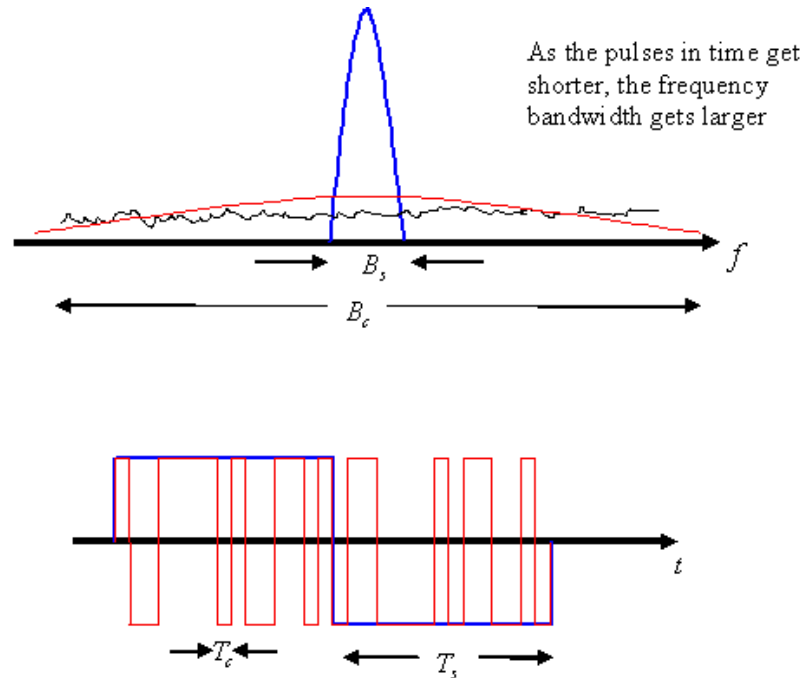
Product Offering

- Gold Code Generator Peripheral
- Used for a variety of secure communication methods
- Widely used in Spread Spectrum Communications
 - Direct Sequence Spread Spectrum (DSSS)
 - Frequency Hopping Spread Spectrum (FHSS)
 - Code Division Multiple Access (CDMA)

Product Offering

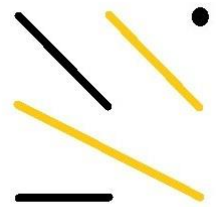


- Direct Sequence Spread Spectrum (DSSS)

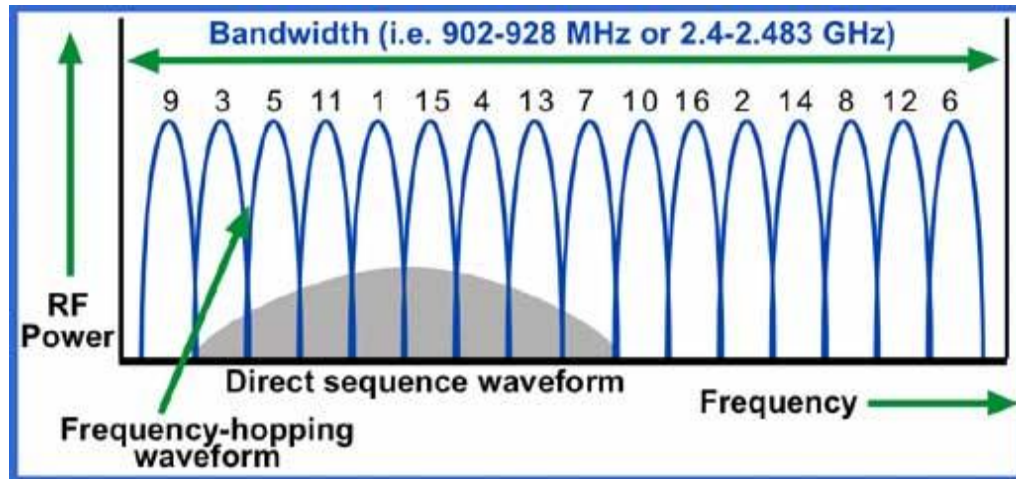


Source: National Instruments

Product Offering

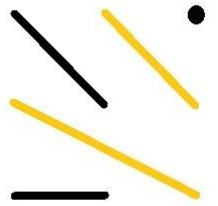


- Frequency Hopping Spread Spectrum (FHSS)

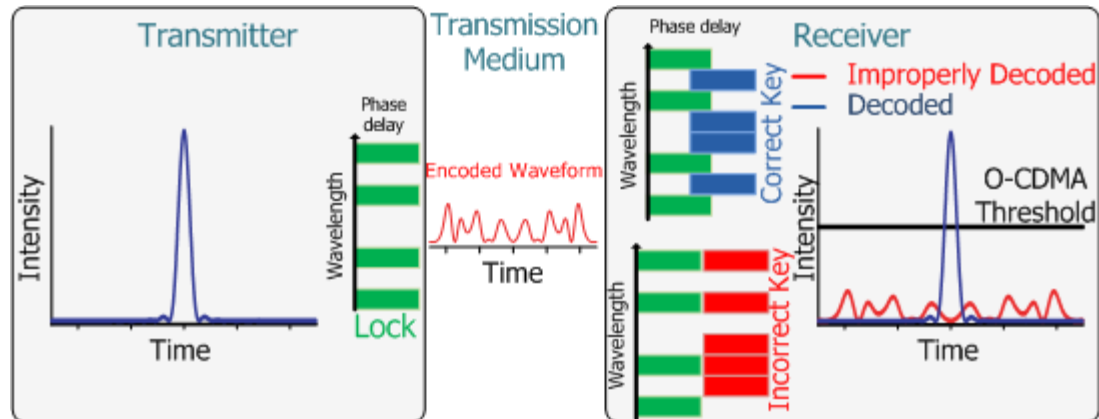


<http://www.data-linc.com/>

Product Offering

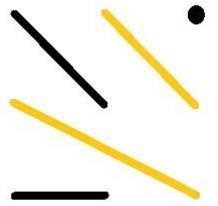


- Code Division Multiple Access (CDMA)

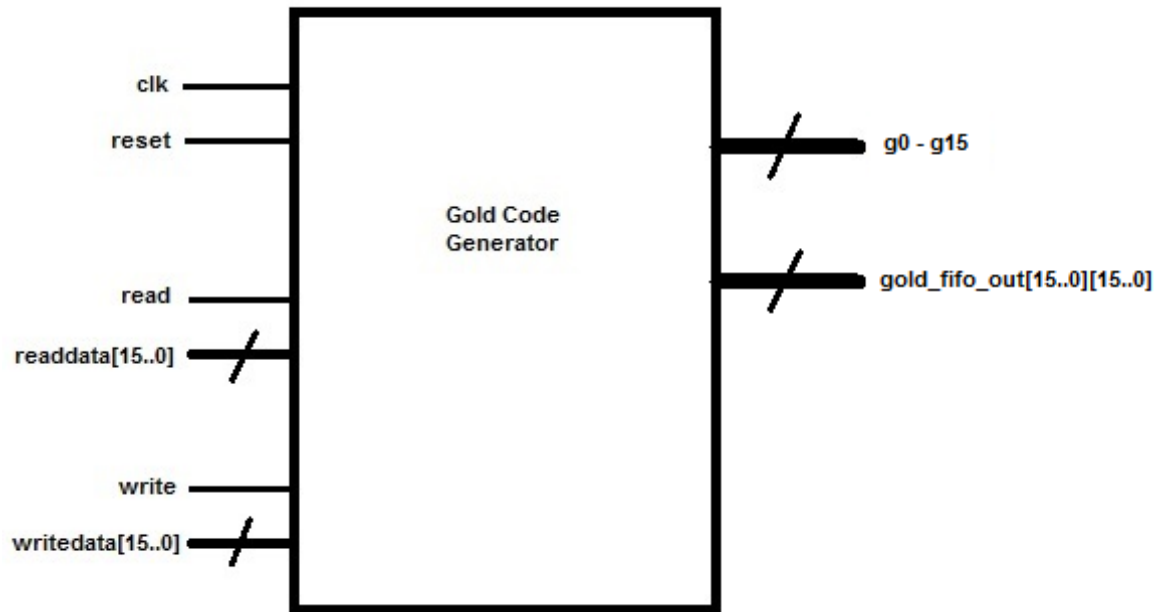


<http://sierra.ece.ucdavis.edu>

Product Offering

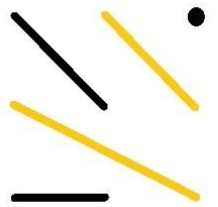


- Aurelii Communications Gold Code Peripheral



Gold Code Generator Block Diagram

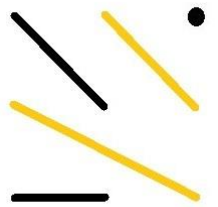
Product Offering



Gold Code Generator Peripheral Features

- 5 bit Fibonacci Linear Feedback Shift Registers
- Fixed 5 bit Register Contents for Pseudorandom (PN) Sequence 0
- Variable 5 bit Register Contents for Pseudorandom (PN) Sequence 1
- 16 Channel Serial Gold Code Output
- Global Output Enable for all Gold Code Channels
- Local Output Enable for all Gold Code Channels
- Global Enable for all Gold Code Channels
- Local Enable for all Gold Code Channels

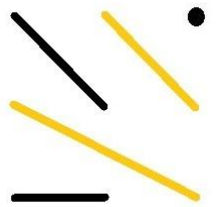
Product Offering



Gold Code Generator Peripheral Features

- 5 bit Address and 16 bit Microprocessor Interface
 - 4 bit PN Sequence 1 Initial Contents
 - 4 bit Control and Status Register
 - 5 bit PN 0 Readback
 - 5 bit PN 1 Readback
 - Global Enable
 - Global Output Enable

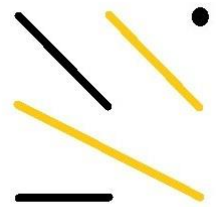
Product Offering



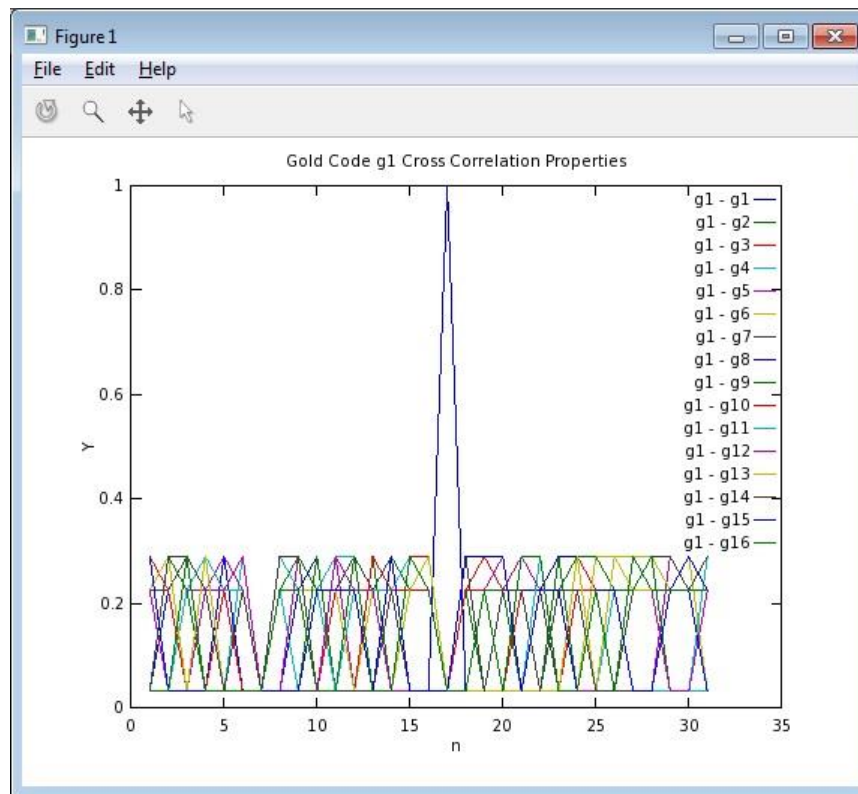
Gold Code Generator Peripheral Features

- 16 bit Output for FIFO Interface
 - 5 bit PN Sequence 0 Registers
 - 5 bit PN Sequence 1 Registers
 - 5 bit Gold Code Registers
 - 1 bit Gold Code Output

Product Offering



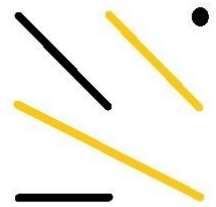
Aurelii Communications Gold Code Peripheral



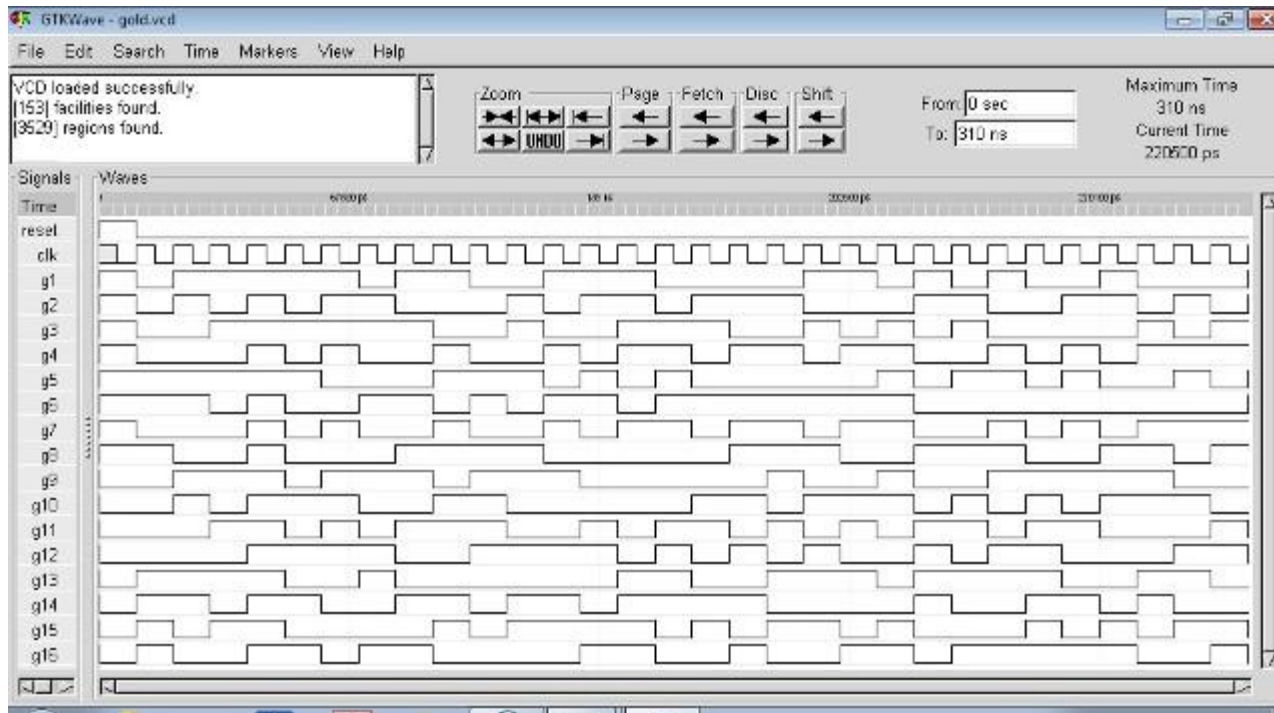
Gold Code g1 Cross Correlation Properties

Proprietary Confidential

Product Offering

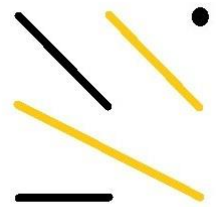


Aurelii Communications Gold Code Peripheral

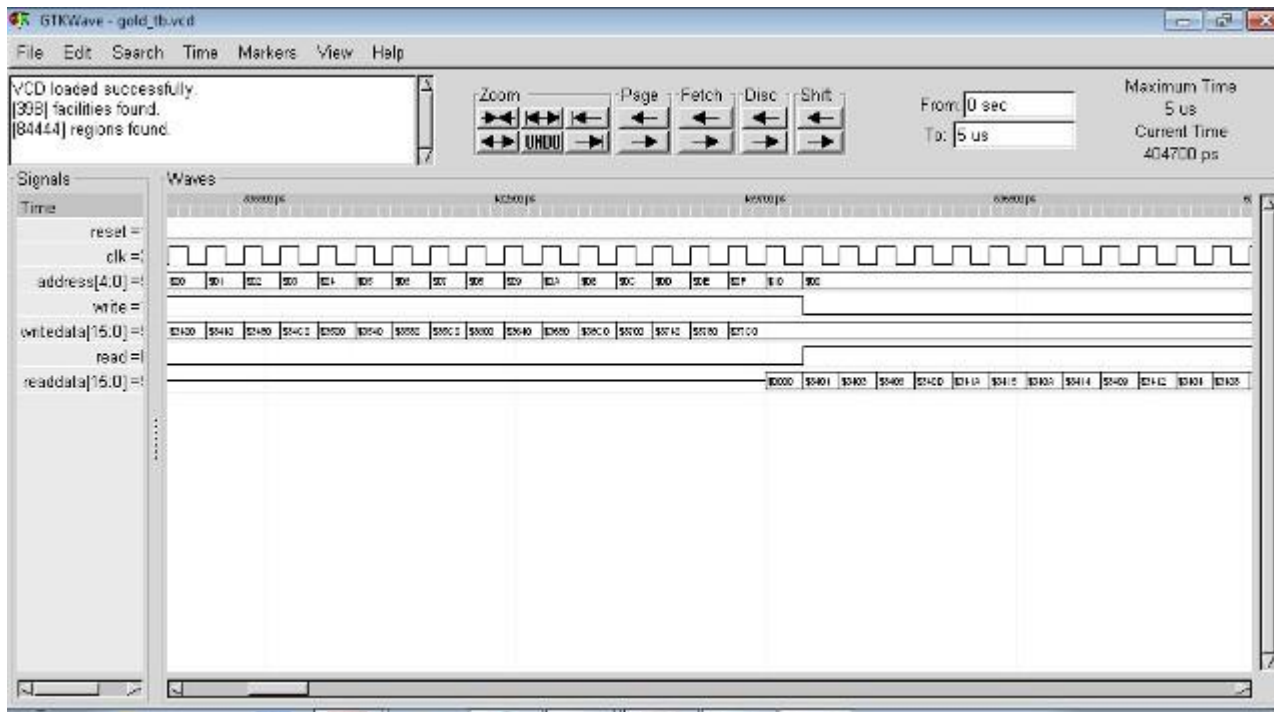


Gold Code Peripheral Output Waveforms (16 Channels – 5 Bit LFSR)

Product Offering

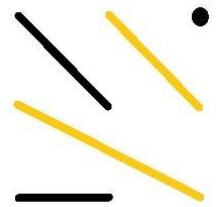


Aurelii Communications Gold Code Peripheral

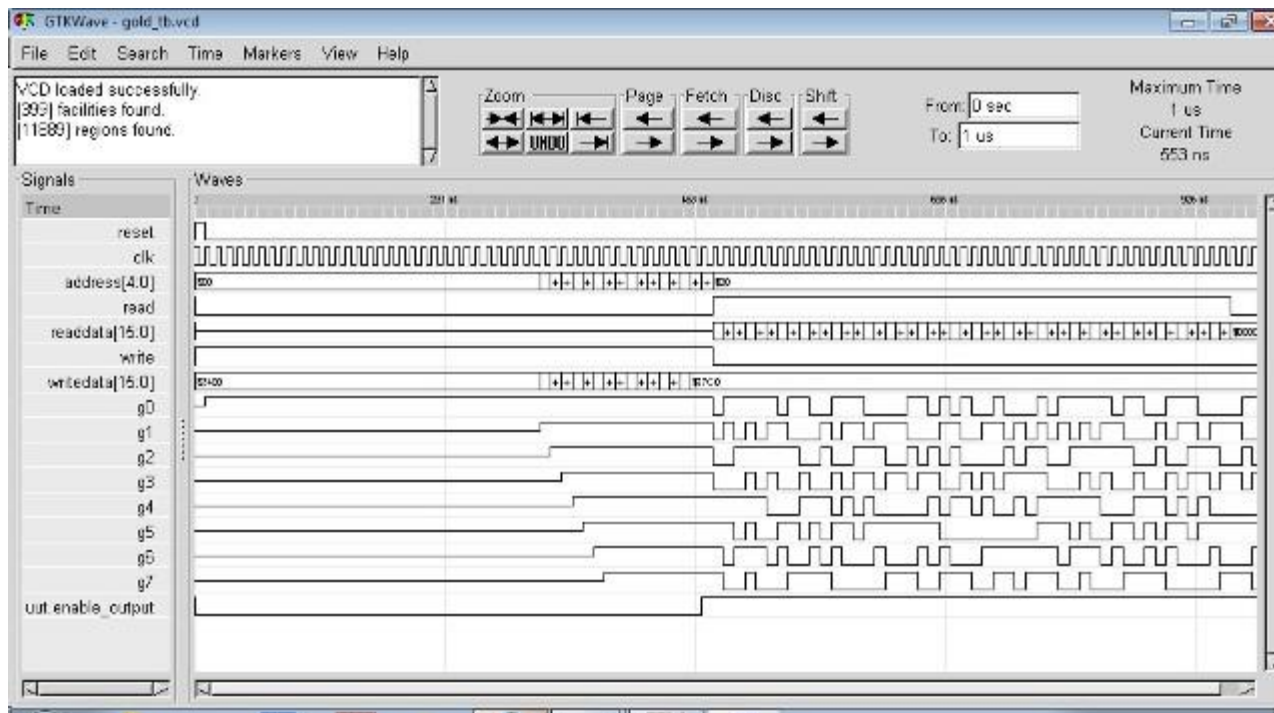


Microprocessor Interface with Read/Write illustrations

Product Offering

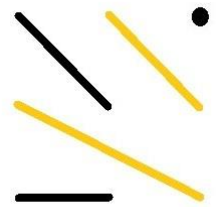


Aurelii Communications Gold Code Peripheral

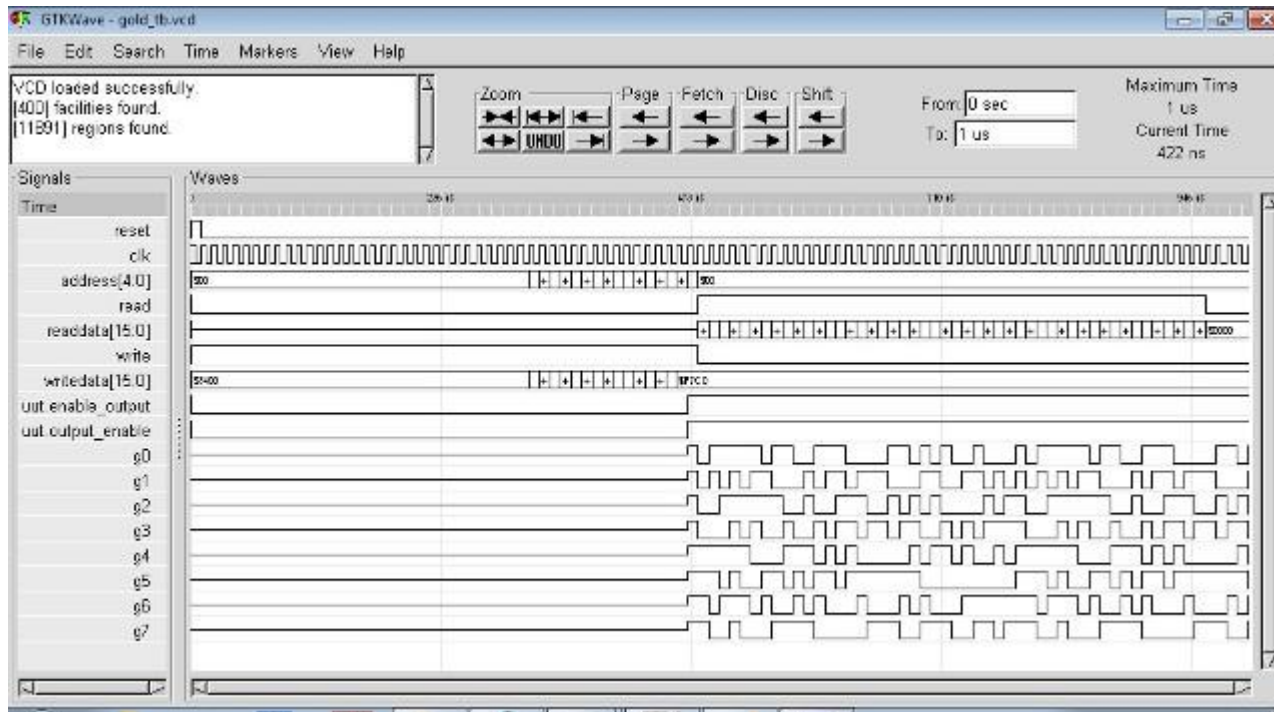


Gold Codes being enabled as a group and tri stated individually

Product Offering

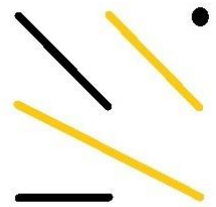


Aurelii Communications Gold Code Peripheral

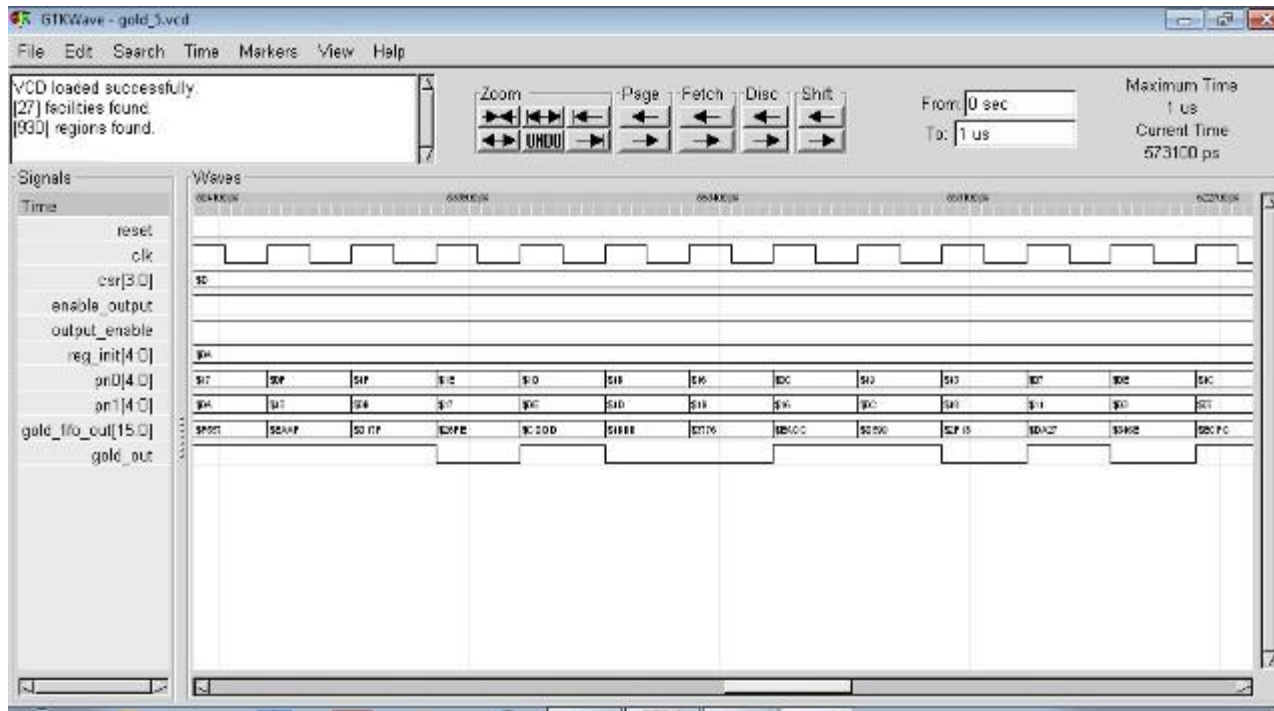


Gold Code channels being tri stated as a group

Product Offering

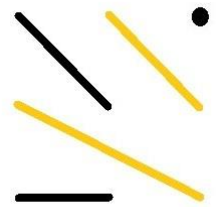


Aurelii Communications Gold Code Peripheral

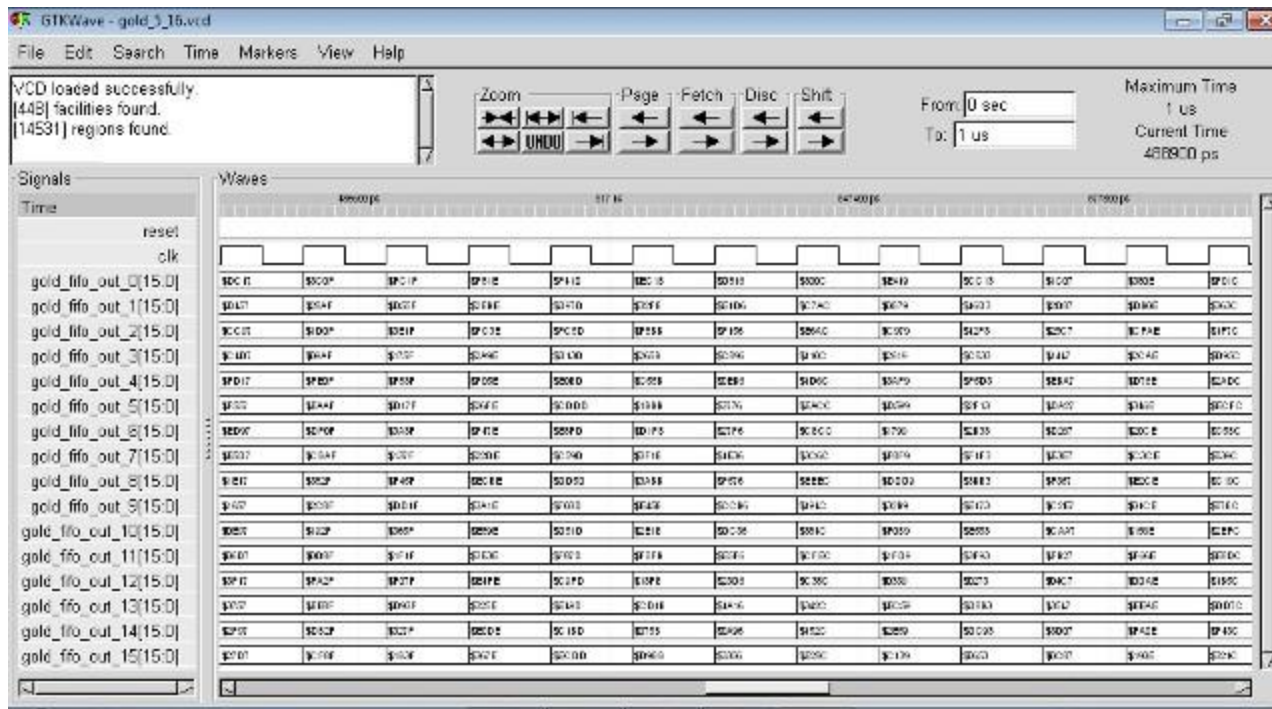


Parallel FIFO Interface – Single Channel

Product Offering

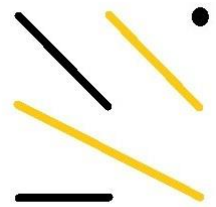


Aurelii Communications Gold Code Peripheral

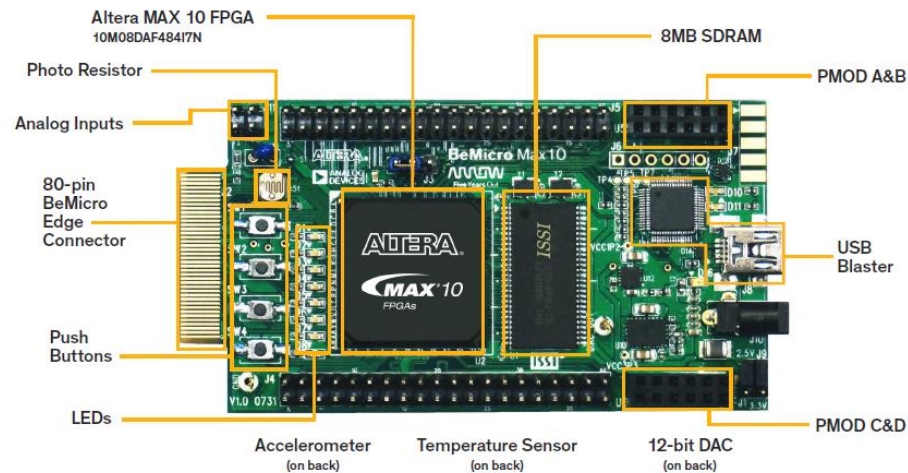


16 Channel 16 bit Gold Code Output FIFO Interface

Product Implementation



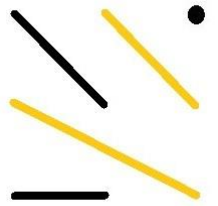
Altera FPGAs



Altera BeMicro MAX 10 Development Kit

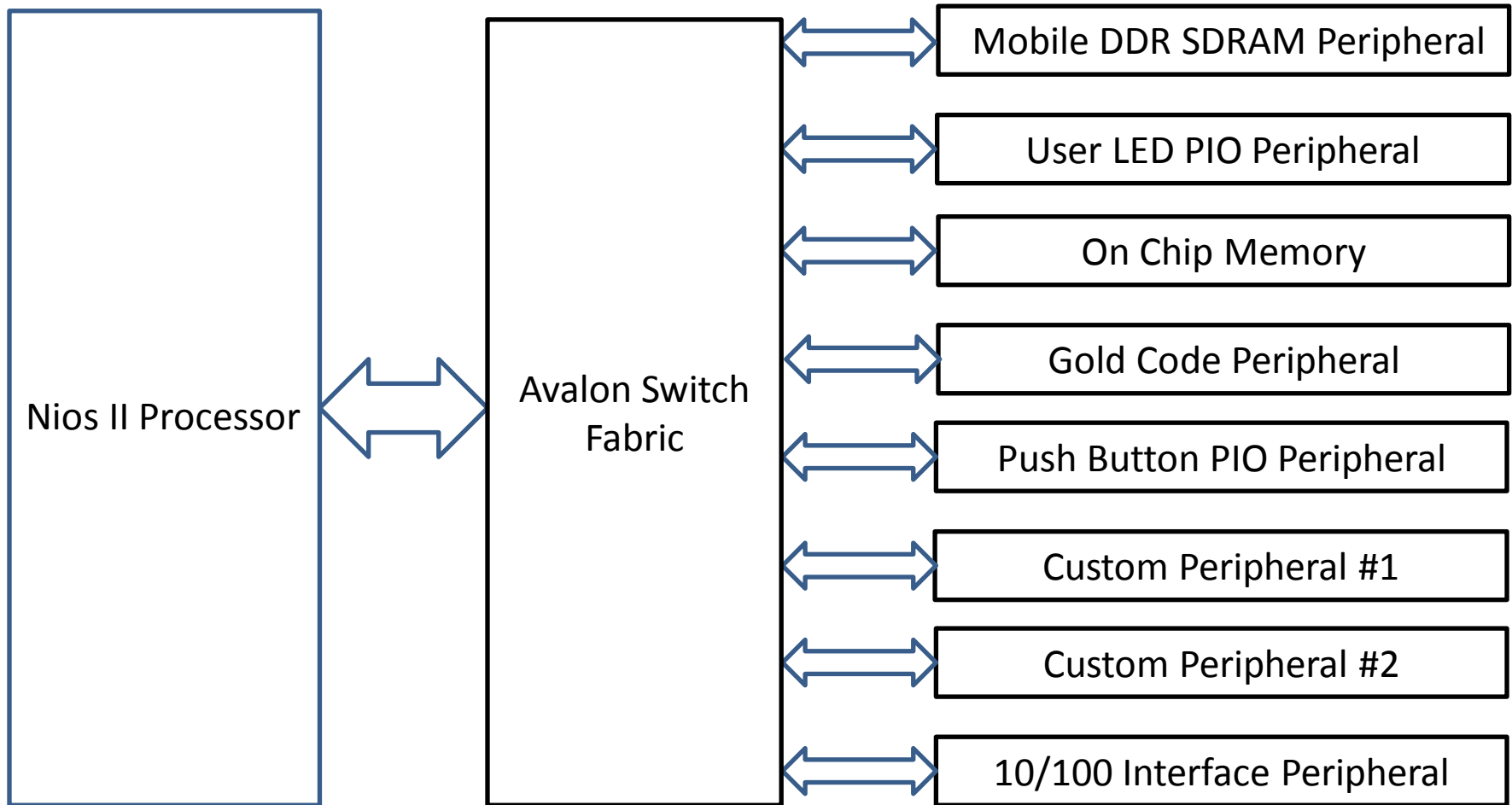
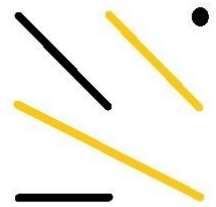
Product Implementation

Altera FPGAs



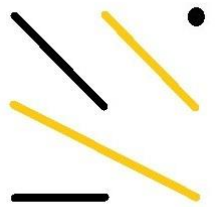
Altera DECA MAX 10 Development Kit

Product Implementation



Example Gold Code Peripheral System

Aurelii Communications



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